



## Yield Learning Solution

**Accelerate time-to-market and maximize entitlement yield using the most comprehensive product based yield analysis solution in the industry.**

The Yield Learning Solution provides on-tester capture and real-time statistical analysis of electrical failures on complex SOC product die, accelerating time to entitlement yield. The solution enables volume yield analysis by efficiently capturing millions of faults per day on testers. This drives efficient collaboration between design, test, in-line inspection, and failure analysis. Yield Learning allows users to more efficiently identify hidden yield loss mechanisms due to design/process interaction and accelerate time to volume production as well as time to entitlement yield.

The Yield Learning Solution provides on-tester capture and real-time statistical analysis of electrical failures on complex System-on-a-Chip (SOC) product die. It efficiently reduces large quantities of electrical failures from probed wafers or packaged parts into specific logical faults. The powerful suite of software analysis and visualization tools enable fast localization of the root cause physical defects, such as: stuck-at defects; timing faults in scan chains and clock trees. The result is significantly faster time to problem diagnosis.

The Yield Learning Solution consists of three elements:

- **On-tester Pre-analysis Module:** With Triage Fault Locator software, large quantities of electrical failure data are efficiently collected on-tester at the wafer sort stage. Using proprietary algorithms, this data is reduced into a more manageable form showing logical faults.
- **Analysis and Visualization Tools:** The YieldVision analysis and visualization tools show the information in wafer maps, die maps and net maps. The data collected can be stacked and analyzed by die, by wafer, by complete wafer lots, or even across multiple lots by identifying faults with statistical significance:
  - Provides prioritization and root cause analysis of the faults which is used to create smart reports. Reports can include histogram data, device hierarchal data, structural data etc.
  - Integration around all of these tools into a single tool set – with standard interfaces to existing processes and tools, including fab defect management systems and yield management systems.
- **Right Test Architecture:** The V93000 SOC test system is engineered with the right test architecture, scalable to meet current and future complex SOC/SIP test challenges, and features the industries first on-the-tester fault localization tool.

Verigy is currently working with early-adoption customers, and the Verigy Yield Learning Solution will be widely available at the end of the year. More information is available at [www.verigy.com/go/yield](http://www.verigy.com/go/yield).