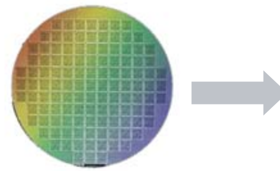
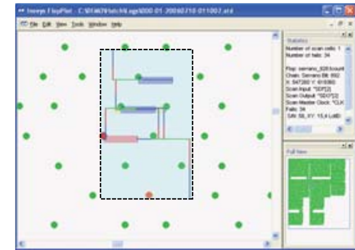
Inovys YieldVision™

Product-based Yield Analysis

YieldVision is a design centric, offline analysis suite that enables real time statistical analysis of electrical defects on product die.



Yield issue observed



Problem diagnosis

YieldVision is our revolutionary layout centric, offline analysis suite designed specifically for volume yield analysis of complex SOC devices with advanced structural test. Yieldvision works with data collected by the Inovys Personal Ocelot™ and Inovys Ocelot ZFP™ tester platforms or with other tester platforms equipped with our Inovys FaultLocater™ pre-analysis module.

Identify and Diagnose SOC Yield Problems Faster

YieldVision provides a comprehensive suite of tools that enables complete characterization of all random, systematic and parametric defects in the process by analyzing the data collected by the primary benchmark of the industry, electrical test. Comprehensive analysis of electrical test data allows detection, assessment and resolution of such difficult defects as resistive metallization paths, Vdd-min problems and weak library cells.

Analysis and Visualization of Test Data

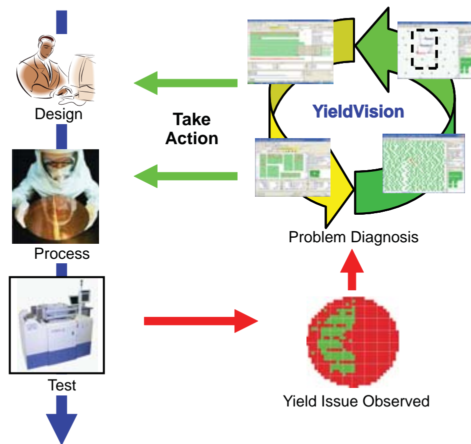
YieldVision provides a layout centric analysis and visualization platform that displays faults and groups of faults in 3 important views. Faults are displayed as a structural view showing the faults in a simple row/column format where each row represents a scan chain and each column represents the bit position in that chain. This view provides the analyst with a logic bitmap view of faults in SOC devices, enabling the type of analysis traditionally limited to memory devices. Faults are also displayed in a hierarchical view showing logic blocks and the design hierarchy. This enables the analyst to focus on specific elements of the design for debug, characterization or yield analysis, enabling parallel efforts on multiple issues without interference. Finally, the faults are displayed in a physical view showing the physical location of the defect on the die. The physical view includes our unique "splat" level view showing specific net trace paths from the failing observation point. This capability enables fast localization of the root cause physical defects, such as: stuck-at defects; timing faults in scan chains; logic; and clock trees. The result is significantly faster time to problem diagnosis.

Key Benefits:

- Efficiently identify previously invisible yield loss mechanisms
- Isolate and physically locate electrical faults in logic, chains and clock trees faster
- Characterize logic speed behind every scan flop
- Easy to use tool to provide yield feedback to process and design.
- High accuracy for the lab
- High throughput for production

- Comprehensive solutions for parametric and systematic defect detection and analysis
- Addresses non-visible defects, layout dependent defects and design weaknesses
- Proprietary AC performance analysis for combinational and sequential logic

Enabling Accelerated Yield Ramps by Closing the Loop Between Test and Fab

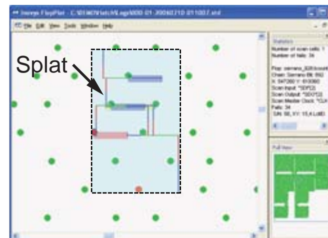


Rapid Isolation of Fault Locations

YieldVision is architected using industry standards to interface with the leading Electronic Design Automation (EDA) tools. A proprietary layout database compiler and extraction engine is then interactively linked with multiple fault analysis modes and visualization tools.

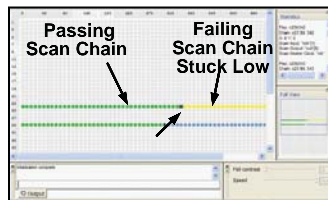
Fault Visualization Tools

Flexible analysis using wafer and die maps is included. Also, physical bounding boxes, or Splats™, are produced to localize each fault to a small area on the die. A Splat shows the failing flop and the path back to the last passing flop. Interconnect metal layer and circuit elements along the path are identified.



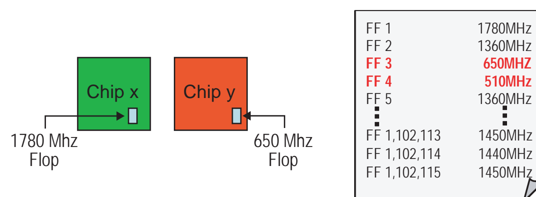
Blocked Chain

Fast analysis of blocked scan chains is provided. Faults may also be visualized as Splats.



SpeedMap Timing Analysis

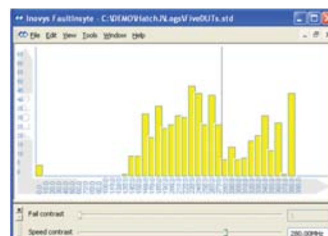
Logic speed behind each Scan Flop across a die may be collected, enabling comparison of parametric deltas across multiple chips or multiple wafers by Scan Flop.



FF 1	1780MHz
FF 2	1360MHz
FF 3	650MHZ
FF 4	510MHz
FF 5	1360MHz
⋮	⋮
FF 1,102,113	1450MHz
FF 1,102,114	1440MHz
FF 1,102,115	1450MHz

Statistical Analysis Tools

Fault data from all failure modes may be stacked and analyzed by single or multiple die – enabling the traditional failure analysis process to move from a singular to statistical approach.



SPECIFICATIONS

Import and View Structural Test Data

- Structural view: By scan-chain structure
- Hierarchal view: By design architecture
- Physical view: By physical layout (wafer or die level)
- Histogram View: Sort by speed

Link to Physical Layout Database

- Provides defect to layout overlay
- Trace functions (Fan in, fan out)
- Generate IP protected trace picture (i.e. Splat)

Track & Filter by Multiple Fail Variables

- Structural Test: Scan chains, bits in chain, scan patterns, pattern set, etc.
- Manufacturing: Program rev, lot ID, wafer ID, facility, XY coordinate, etc.
- Pattern Content: execs, bursts, specs, test IDs, etc.

Powerful GUI for Visual Variables

- Zoom to any level of detail within View
- Adjust color thresholds to filter failures by numerical intensity
- Intuitive displays show complete design data on any hierarchy or bit cell

Interfaces with Leading Tools, Including:

- Mentor Graphics FastScan™
- Synopsys TetraMAX™
- Cadence Encounter™
- YMS through KLA Results File (KLARF)

PC Based

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