



Verigy V6000 FT

Product Overview

Industry Challenges

IC prices and production levels have fluctuated dramatically in recent years, bringing into stark relief the entire industry's volatility. In response, manufacturers must prepare for any change, any challenge, at any time. The current ramp-up in memory testing capacity must be made responsibly.

In particular, sustainable competitiveness requires manufacturers to:

- Minimize cost of test through high parallelism and low downtime for repair and maintenance
- Maximize utilization of capital investment by flexibly testing multiple DUT types, even across a range from high volume / low device mix to low volume / high device mix

Now, for the first time, with V6000 FT, the scalability, flexibility and high parallelism provided by Local Pin Electronics technology is available for final test.



V6000 FT is a scalable and flexible high-parallelism solution that allows manufacturers to meet the diverse final test needs of DRAM, Flash and MCP with low cost of test.



Product Summary

Benefits of Local Pin Electronics now available for final test on V6000 platform

The multiple benefits of Local Pin Electronics (LPE) are now available for final test on the V6000 platform. Since 2008, LPE technology has brought the tester pin electronics to the devices under test. This improves electrical performance by eliminating long electrical distances that attenuate device signals, providing better test yields while reducing tester per-pin cost. LPE technology also enables the V6000 interfacing design to flexibly adapt to the mechanical requirements of handlers.

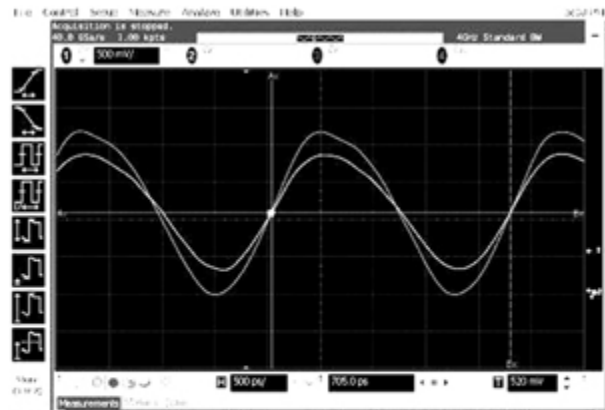
Because of its all-I/O, Tester-Per-Site architecture, the V6000 FT is ideal for multiple device types (MCP, DRAM and NAND) and multiple test scenarios, from low to high product mix, and from low to high volume. Such flexibility is the key to achieving higher tester utilization, greater throughput and lower cost of test. Utilization is boosted even more because all pins support I/O testing requirements. Test cells can be designed around the needs of each device type and handler, not around the limitations of the tester.

The V6000 FT's flexible architecture eliminates the interfacing drawbacks found with more rigid tester technologies, which require expensive and bulky test fixtures. Interface components are modular and lightweight, meaning that routine maintenance, such as replacing a worn socket, can be done in seconds, thus with minimal downtime. When one device design is no longer produced, many interface components are reused for the next design to lessen environmental impact.

Better yields through improved signal integrity by placing LPE physically closer to the DUT

With approaches based on conventional test fixtures, the extended distance of wires between the socket (containing the DUT) and traditional test head pin electronics leads to a degradation of signal integrity, which brings down yields. With V6000 FT and LPE, that distance is only 10 cm. As a result, testing at

up to 880 Mbps, signal integrity and, therefore, yields are better. For device pins that do not require as high signal integrity, driver sharing can still be used (also with better signal fidelity than traditional remote pin electronics), further lowering cost of test.



- 440 MHz signal as seen:
- 18 cm from the driver (V6000)
 - 67 cm from the driver (Traditional trace)

LPE Signal Fidelity Advantage

Multiple dimensions of cost brought down through flexible LPE architecture

LPE architecture provides high pin count at reduced cost per pin. Fewer test cells require less floor space and therefore lower costs. Industry-leading power and cooling management further reduce cost.

Conventional test fixtures dedicate one specific interface for each device type at final test, thereby requiring additional capital expense for each device type. Additionally, these fixtures must be manually swapped out for maintenance (for example, as test sockets wear out) or to test a new device type. Swap time is downtime, and in a high mix environment swaps could be frequent, diminishing throughput.



Local Pin Electronics (LPEs)

In contrast, the V6000 FT interface, enabled by LPE and an all-I/O architecture, replaces the test fixture with a set of Individual Load

Boards (ILB), which are each easily swapped out by a single operator in just seconds. A new device type requires only a new ILB. Shifting to a new handler parallelism requires only a minor mechanical change to reposition the LPEs to match the new handler pitch.

Cost-effective for broad range of test scenarios

The V6000 FT's flexible architecture makes it well suited for a broad range of testing scenarios, from low device mix, high-volume testing (such as commodity DRAM or Flash) to high device mix, low volume testing (including specialty devices and MCPs).

Because of the time and cost involved in swapping conventional test fixtures, plus the high capital expense of multiple fixtures, these approaches are problematic for low volume, high mix scenarios.

Simpler, faster and less costly fixture maintenance

Conventional test fixtures require complicated and expensive maintenance, even in high volume / low device mix scenarios. When sockets wear out, the bulky fixture must be entirely removed, which is slow, requiring several operators. Given these drawbacks, the test engineer may delay replacing sockets, choosing instead to take them out of service, which diminishes utilization and throughput.

The V6000 FT avoids these problems altogether with its modular design based on the Independent Load Board (ILB). When a socket needs to be replaced, the operator unlatches the specific ILB and makes the change in 30 seconds. The result: minimum downtime, maximum utilization and throughput.



It is easy to replace a socket with the Independent Load Board

In addition, in contrast to the cost and space requirements of keeping spare test fixtures on hand, spare interface inventory is easily assured with a small number of far smaller components.

Lower environmental impact with V6000 FT's modular design

Conventional test fixtures are custom-configured and dedicated to testing a particular device. Once that testing is completed, the large and bulky fixture must be discarded.

The V6000 FT's modular design minimizes waste. Of the three components - socket, metal frame, and circuit board - the socket and metal frame are reused across device types. Only the circuit board needs to be recycled.

Optimal parallelism and lowest cost of test because of flexible architecture and multipurpose (all-I/O) pins

Conventional test fixtures are hardwired for one particular device, meaning the interface cannot be repurposed, or adjusted to seize a higher parallelism opportunity. If the tester is used for a new device, the fixture must be replaced, and any inflexible tester pins (drive only) can reduce the tester utilization for the new device.

Additionally, unlike testers where pins may be designated drive-only or I/O, all V6000 FT LPE pins are I/O, for optimal tester utilization. This allows maximum pin utilization to achieve the optimal parallelism presented by each test scenario. For example, you might achieve 256 test parallelism when required for one particular device, but then quickly reconfigure to achieve 384, 512 or 768 parallelism for another particular device. With the scalability of the V6000 FT, parallelism is limited by the handler or test strategy, not by the tester.

Lower risk provided by flexible, scalable architecture that adapts to changing marketplace

While the V6000 FT can be configured for lowest cost of test for a particular device, its architecture allows for optimal testing of a broad range of devices. A tester with a device-specific dedicated architecture will

become inefficient as production changes over time. When responding to shifting production strategies, the V6000 FT can be reconfigured to re-optimize for whichever memory device is demanded.

Features and Benefits

FEATURE	BENEFIT
Local Pin Electronics (LPE)	Short distance between pin electronics and DUT, preserving signal integrity for better yields
All-I/O, Tester-Per-Site architecture	All pins in the LPE test head support I/O testing requirements, for higher tester utilization. V6000 FT is ideal for multiple device types (MCP, DRAM and NAND) and multiple test scenarios, from low to high mix, low to high volume, and single pass to dual pass.
Modular Independent Load (ILB) Board design	Replaces conventional test fixtures. A worn socket can be replaced in seconds, minimizing downtime while maximizing utilization and throughput. Lowest consumables cost.
Reusable components	Sockets and metal frames are reused, not discarded, which reduces the environmental impact.
Best in class power/cooling efficiency	Lowest operating costs

Key Specifications

SPECIFICATION	VALUE
Test sites	128 max (32 TSMs max)
Tester resources	18,432 I/O pins, 2,048 DCV max
Power supply outputs	4096 Max
Test frequency / Data Rate	280 MHz / 560 Mbps (+/- 30 ps) LPEs 880 Mbps (+/- 30 ps) 140 MHz / 280 Mbps (+/- 400 ps) 70 MHz / 140 Mbps (+/- 1 ns)
ECR	Up to 64 Gigabits per Test Site Module
Applications	NAND, NOR, DRAM, SRAM, MCP

Related Information

For more information about the V93000 Direct-Probe Solution, please visit the following website:
www.verigy.com/go/V6000

Contact Information

For more information about the V93000 Direct-Probe Solution, please contact your local Verigy sales representative. **www.verigy.com/go/contactus**

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