



Testing DisplayPort v1.2 at 5.4Gbps on PS3600

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Abstract

Purpose of this paper is to show how devices manufactured to DisplayPort 1.2 specification can be tested at full speed (5.4 Gbps per differential lane) on PS3600.

V93000 PS3600 is established in significant quantities throughout the supply chain of our customers. Nominal rating of the PS3600 is 3.6Gbps. Nevertheless, the analog bandwidth of the PS3600's receiver does permit going for a higher speed. Typically, the analog bandwidth of a channel receiver is sufficient for a reliable test of a clock signal at around 6Gbps with a damping factor close to -6dB.

By applying of some techniques shown below (dual pass, quad pass with level shift), available bandwidth of PS3600 can be used in order to perform at-speed testing of a DisplayPort transmitter at 5.4Gbps in production.

1. Mini-review of DisplayPort

Continuous increase in digital display sizes, break-through of FULL HD and 3D capable hardware requires higher resolution, higher frame rates and higher color depth in order to maintain and improve picture quality. Lossy compression algorithms are usually not an option since the quality degradation is noticeable. With high color depth of 16bit per color channel, raw data rates of more than 10 Gbps are already being used by Digital Cinema 2K standard [Figure 1], and data rates way beyond that are required by coming 4Kx2K standard.

Name	Horiz.	Vert.	Colors	Approximate Bandwidth
HDTV/ Blu-Ray	1920	1080	36	7 Gbps
Digital Cinema 2K	1998	1080	48	> 10 Gbps

Figure 1: Established resolutions and associated data rates

In order to cover this demand for a new generation of high-speed digital video interface, VESA (Video Electronics Standards Association)^[1] established a license-free interface standard, DisplayPort,

capable of transmitting both Audio and Video information and scalable in bandwidth (up to 4 single lanes can be combined to transmit the data). DisplayPort is intended to become a successor for outdated DVI port and notebook-internal LVDS connections, for fixed pixel displays in a computer industry, and for home entertainment. It features such characteristics as mechanically stable compact and lockable connector, fewer single lines with embedded clock, additional bi-directional channel for scalable inter-device communication, and overall scalability and option for easy standard extensions [Figure 2]. DisplayPort is further more flexible in supported resolutions and color depths compared to competing HDMI standard widely spread in home entertainment industry. First specification of DisplayPort has been published in 2006, with specification 1.1 following in 2007 [2].

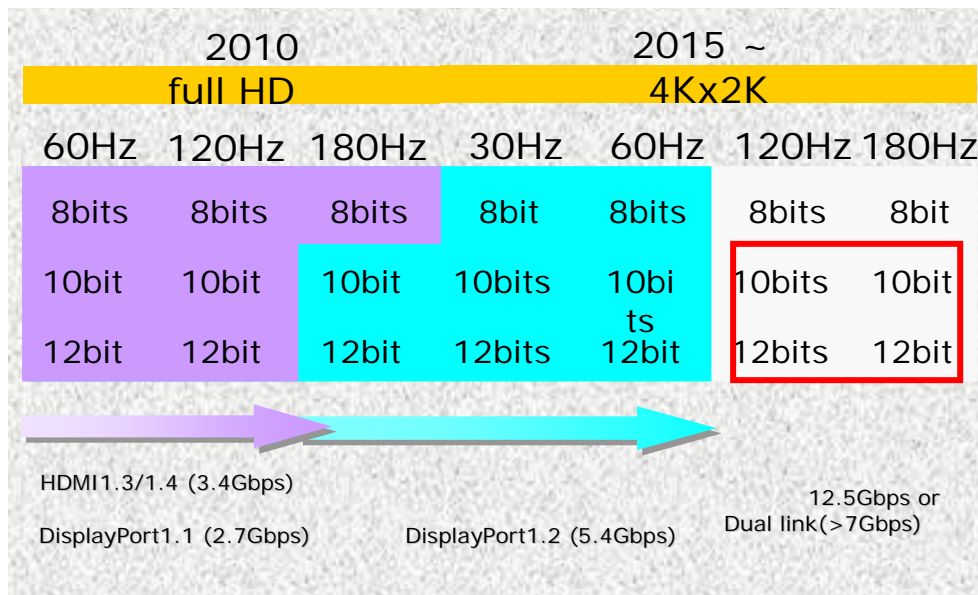


Figure 2: Resolution and bandwidth requirement trend [3]

2. DisplayPort 1.2 – characteristics and features associated with Transmitter Test

Specification of DisplayPort 1.2 released in August 2009 allows for up to 4 differential unidirectional lanes combined to a Main Link [Figure 3].

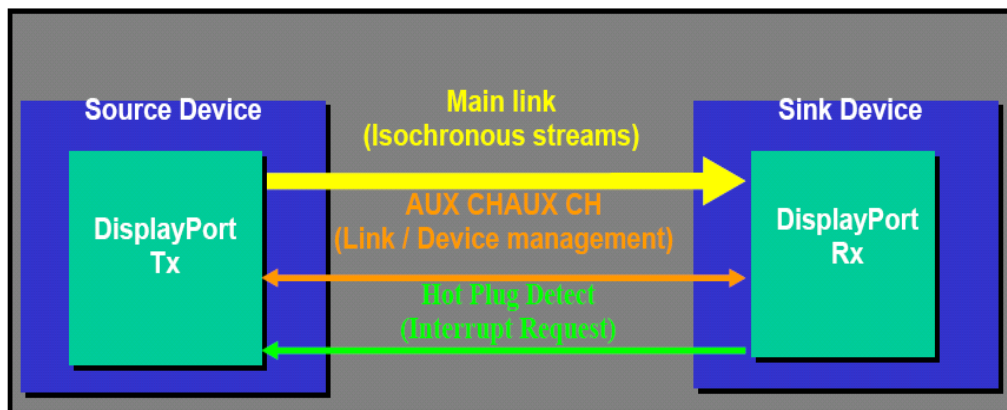


Figure 3: Communication channels of DisplayPort [3]

Each lane can carry audio and video streams at a symbol rate of up to 5.4GBd. Although in the application it is important to differentiate between the actual data rate of 4.32Gbps per lane vs. symbol rate of 5.4GBd (an ANSI-8B10B modulation is being performed for data transmission), the difference is negligible for the topic of this paper, and both terms are therefore used interchangeably. The Video/Audio signal protocol of DisplayPort is compatible neither with HDMI nor with DVI. Graphics card manufacturers use a trick in order to offer simple low-cost mechanical DVI/HDMI-DisplayPort converters: the graphic card determines whether a converter is attached, and is switching the protocols on-the-fly accordingly.

Apart from Main Link, DisplayPort possesses a low-latency constant-bandwidth auxiliary link AUX CH to allow half-duplex bidirectional communication. This channel can be used for information exchange with touch-screen displays, for transmission of USB protocol data, for cameras, microphones and other peripheral equipment.

An additional connection is used for hot plug detection.

The 4 lanes of DisplayPort transmitter are skewed against each other by two LS_Clk (Line Symbol Clock) cycles in order to reduce the sensitivity against external noise [Figure 4]. Apart from that, there is a non-deterministic delay before the first data bit is being sent.

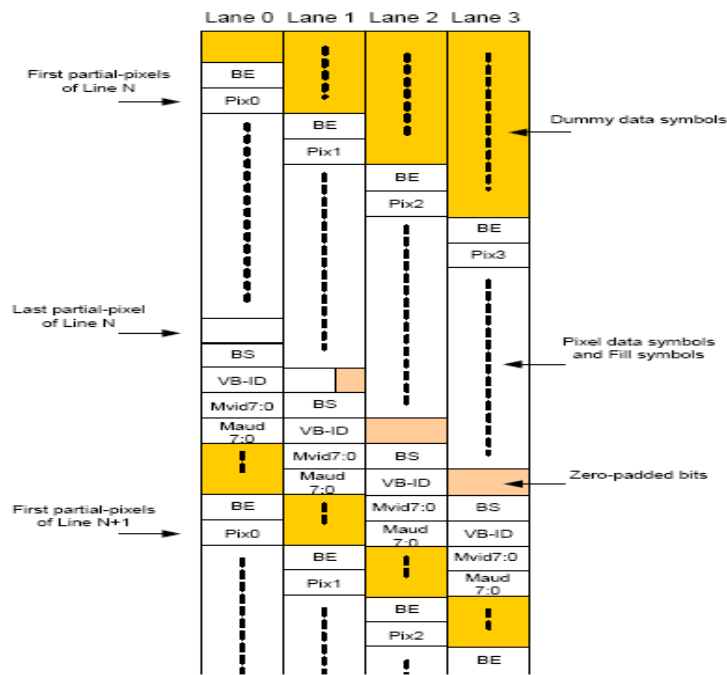


Figure 4: Inter-Lane skewing^[4]

In the actual application, establishing communication requires data training (link training) between transmitter and receiver on every lane. For transmitter test with ATE, a non-deterministic delay on a lane turns a straight-forward single functional test approach impossible. At least the position of the first data edge needs to be determined in order to adjust ATE's timing. This timing adjustment can be still achieved faster than going through the full data training cycle.

DisplayPort offers a link quality measurement feature which allows testing the transmitter in 3 different modes^[4]:

- *Nyquist pattern* – D10.2 symbol unscrambled to provide clock signal on a main link with highest speed (2.7 GHz for 5.4Gbps)
- *Symbol Error Rate measurement* - Bit pattern 00h through scrambler with special reset procedure of scrambler with symbol error count internally
- *PRBS7 pattern* – transmits PRBS7 sequence

Neither of the link quality test patterns requires previous data training, and the pattern will loop unless it has been aborted.

When using ATE for transmitter test, one of these patterns is turned on. The first step for ATE is to synchronize with the pattern in the timing domain. Since the initial delay before the first transmitted bit is unknown and the lanes are skewed to each other, a search must be performed by ATE in order to lock to the pattern.

Acceptable Diff peak-peak amplitude of the output signal is between 0.4-1.2V. For high speed test of the link, the output should be programmed to V_{diff} 1.2Vpp to ensure best signal integrity across the signal path.

One of the usual at-speed Main Link tests of DisplayPort 1.1 transmitter at 2.7Gbps performed on ATE equipped with PS3600 includes a search for a rising and falling edge. In this case, a link quality test patterns supplied by transmitter is being used in order to determine the data eye width and its compliance with the specifications.

Usual failure pattern of the transmitter during at-speed test is either stuck output (no data being transmitted at all) or some bits inverted during transmission. Evaluation of production data collected by manufacturers of DisplayPort devices shows that failing of this test due to a min. eye width violation is atypical, as the headroom of the specification is very high at 70% min. data eye width [Figure 5].

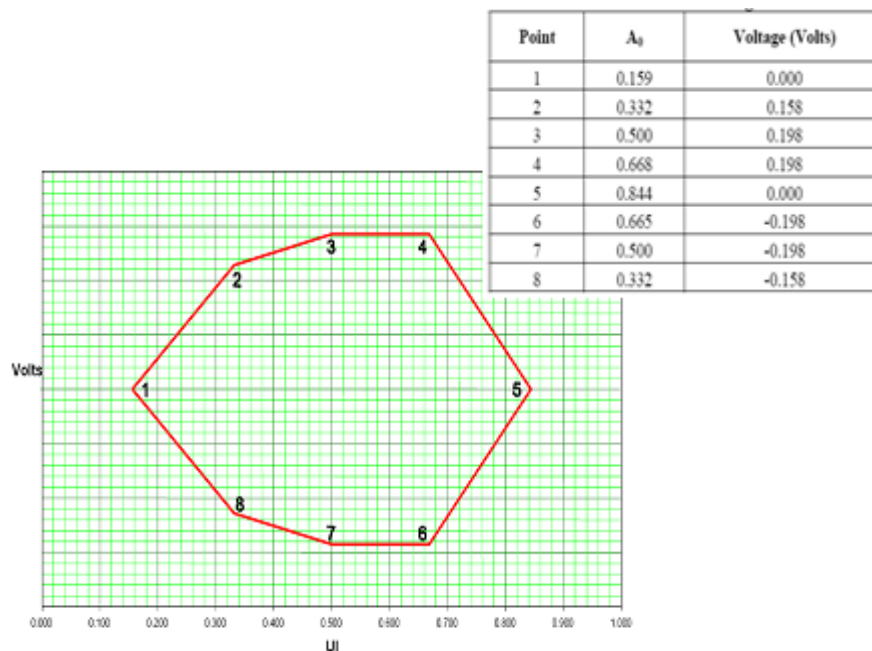


Figure 5: Main Link Eye Mask of Driver^[4]

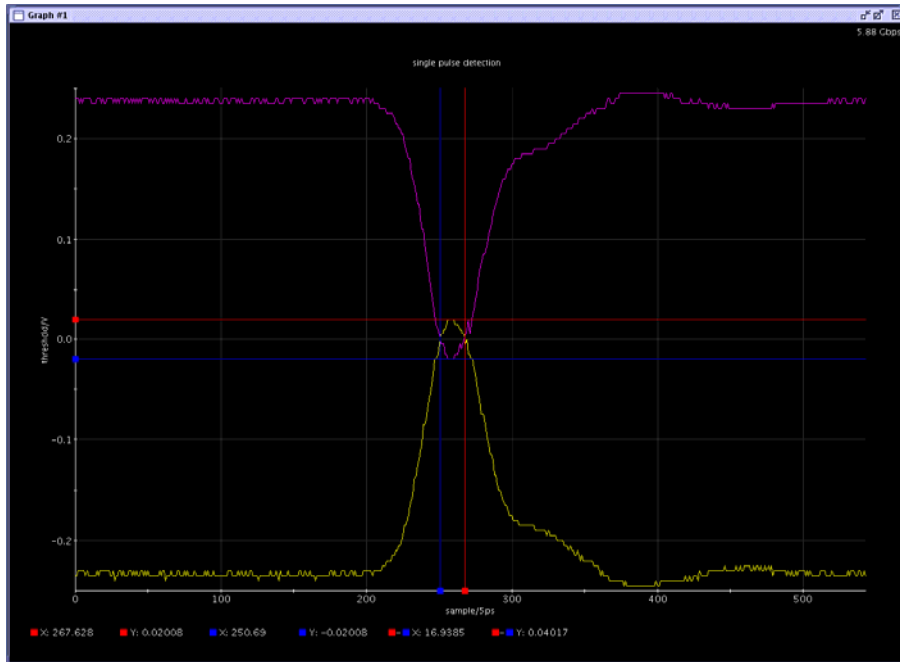


Figure 8: Limited eye opening with a single pulse

As one can observe in the figure above, with a single threshold of the receiver, the remaining margin would not allow for a stable test result. This problem can be overcome at cost of test run time, by further doubling the amount of shots.

The basic approach for a PRBS pattern test is the same as for clock pattern, with following modifications:

- for a first timing search, only 'Compare to H' events are allowed in a pattern. 'Compare to L' events should be masked out. This will allow placing the compare level threshold with an offset to an actual middle of the data eye. Shifting the threshold below the eye center for 'Compare to H' events will provide a larger margin and therefore a more stable test results [Figure 9]. Pattern speed should be 2.7Gbps.
- second step should be performed with the same timing that returned a stable pass at first test, but this time only 'Compare to L' events are allowed, others should be masked out. Now receiver's compare threshold should be shifted again, this time above the center. It is sufficient to perform this test as a single shot, since proper timing has been already determined in a first step
- step 3 is similar to the first one, with a difference that no timing search needs to be performed. Since timing has been already adjusted in a first step, step 3 will require a timing shift by 1 UI, or 185ps. Only 'Compare to H' are allowed. Single shot should be performed
- step 4 is similar to a second one and is using the same timing as step 3. Here again only 'Compare to L' events are allowed.

With such quad pass test approach and provided low levels of jitter on transmitter, PRBS7 generator of DisplayPort can be used along with clock patterns for functional testing.

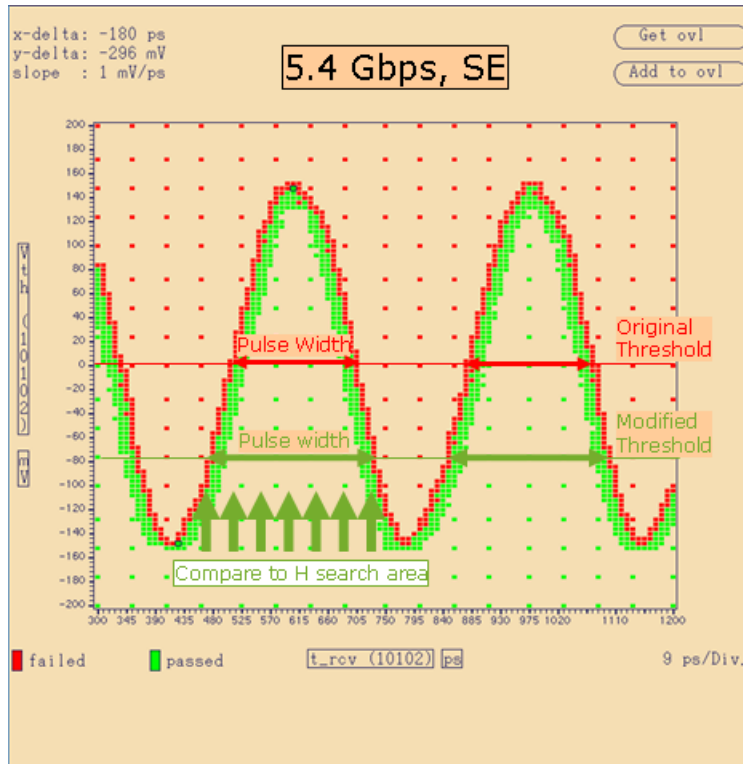


Figure 9: Using shifted threshold for achieving better margins

4. Conclusion

With next iteration of DisplayPort specification, new devices requiring high-speed test at data rates of up to 5.4Gbps are hitting the market.

V93000 Pin Scale 3600 digital card with its superior design and analog bandwidth exceeding specifications can offer a solution for at-speed HVM transmitter test when some boundary conditions described in this paper are met.

5. Acknowledgment

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6. References

- [1] <http://www.vesa.org/>
- [2] <http://www.displayport.org/>
- [3] "DisplayPort Application Introduction", Oliver Guhl
- [4] "DisplayPort Specification v.1.1", VESA