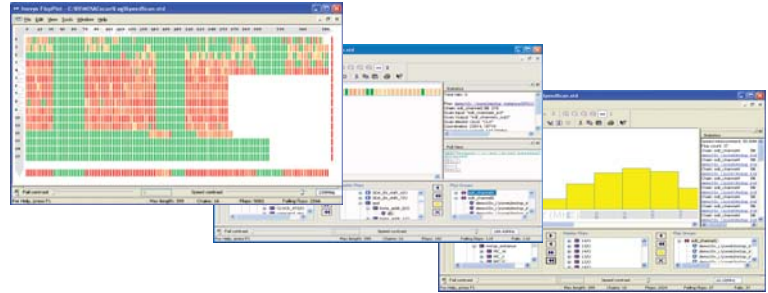


SpeedScan™ and SpeedMap™

Device Performance Characterization with AC Scan



A unique combinational toolset, SpeedScan and SpeedMap use AC Scan techniques for identifying Path Delay and Transition Delay faults on complex SoCs.



Identify and Diagnose Device Design Problems Faster

The challenges to achieve successful debug of new semiconductor designs are compounding, including: Increasing gate count & density; New technology nodes; Decreasing external access; and Increasing defect and fault mechanisms. The response to best address these challenges is implementation of Design For Test (DFT) and leveraging structural test methodologies. Large, complex semiconductor devices such as ASICs and SoCs can generate immense amounts of structural test failure data, which can be very difficult to interpret and analyze. The Inovys FlopPlot toolset manages these large volumes of data efficiently and converts them into easy to understand formats and graphical displays. SpeedMap is the latest addition to the analysis tools available with FlopPlot. This powerful suite of software tools enables DFT, Test, and FA engineers to quickly identify and resolve failures in even the most complex devices, that contain millions of gates.

Achieve Device Performance Characterization with AC Scan

New complex SoC devices using sub-90nm processes exhibit more than simple stuck-at fault models. AC Scan patterns are being deployed in both engineering and production for at-speed testing. However, identifying the source of speed related problems continues to be a challenge for engineers. SpeedScan and SpeedMap enables datalogging from inside the device, yielding timing performance information about the logic behind each and every flip-flop in the scan chain.

Efficient Device Data Collection with SpeedScan

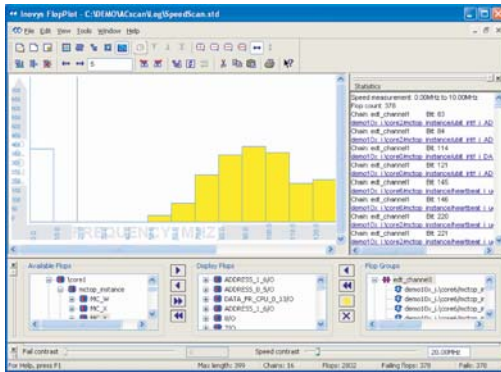
SpeedScan is the device data collection engine that resides on the Inovys test platform, which significantly simplifies the complex process of retrieving the timing performance behind every flip-flop using a single easy to use tool. The user selects whether the characterization is to be performed in the time or frequency domain and the Start and Stop parameters. The Launch and Capture clock attributes are selected from drop-down menus populated from Pattern Exec context. SpeedScan calculates the necessary timing values for each step of the sweep and datalogs results on a per flip-flop basis, even for designs with millions of flip-flops. Progress is displayed with a color spectrum of the number of failing flip-flops at each test point on the sweep.

- Device performance characterization with AC Scan
- Efficient device data collection engine
- Identify DFT speed related failure patterns in first silicon faster and easier
- Track and review failures by individual or multiple devices

Key Benefits:

- Identify and diagnose device design problems faster
- Achieve device performance characterization with AC Scan
- Efficient device data collection with SpeedScan
- Analyze structural performance by flip-flop
- Analyze circuit performance by flip-flop
- Statistically bin flip-flops by performance

Device Performance Characterization with AC Scan



Histogram View >

Analyze Structural Performance by Flip-Flop with SpeedMap — Structural View

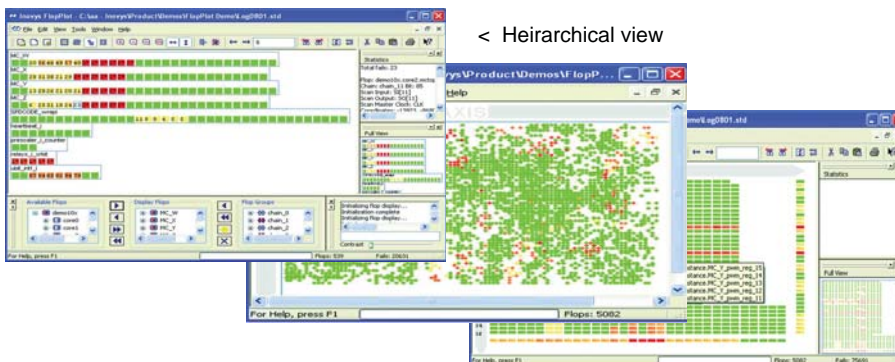
Failing flip-flops are viewed with user defined Fail and Speed contrast resolution. Structural test results generate complete pattern, chain, and bit information for better problem solving and fast debug. Users can dial a frequency to get a color spectrum display for each flip-flop as they are stitched into their scan chain. The Speed contrast slider controls the failure frequency display.

Analyze Circuit Performance by Flip-Flop with SpeedMap — Hierarchical View

The “Hierarchical View” mode enables users to view failures by functional behavioral blocks – start from a core-level and zoom down to the lowest-level design module. In the hierarchical view mode, frequency performance can be observed by filtered circuit. Once a filter is applied, SpeedMap can transform and display the same information as scan chain data (the “Structural View”) or as a relative die plot (the “Physical View”).

Statistically Bin Flip-Flops by Performance with SpeedMap — Histogram View

In the histogram view mode, distribution of flip-flop performance is displayed in user defined bins. Flip-flops that fail at all frequencies can be easily identified—may be caused by False Paths or Multi-Cycle Paths. Flip-flops that do not meet timing criteria can be easily identified to perform further extensive analysis on each path in the logic cones leading to the flip-flops. Essentially, this provides the engineer the ability to find the needle in the haystack.



< Hierarchical view

SPECIFICATIONS

Import and View Structural Test Data

- Structural view: By scan-chain structure
- Hierarchal view: By design architecture
- Physical view: By physical layout
- Histogram view

Track & Filter by Multiple Fail Variables

- Structural test: Scan chains, bits in chain, scan patterns, pattern set, etc.
- Manufacturing: Program rev, lot ID, wafer ID, facility, XY coordinate, etc.
- Pattern content: Execs, bursts, specs, test IDs, etc.

Powerful GUI for Visual Variables

- Zoom to any level of detail within View
- Adjust color thresholds to filter frequency display
- Intuitive displays show complete design data on any hierarchy or bit cell

Direct Links with Leading ATPG Tools, including:

- Mentor Graphics FastScan™
- Synopsys TetraMAX™
- Cadence Encounter™

PC-Based with UNIX Links

- Inovys DiagLink™ connects FlopPlot to UNIX-based ATPGs
- Automated scripts enable remote management of long diagnostic jobs via CygWin interface
- Runs on any Win2K or WinXP PC