



Functions and Features of Verigy's new HSM6800 Pin Electronics Card to test High-Speed Memory Devices

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Abstract

In the recent past, high-speed memory devices adopted a growing amount of I/O-architectural features from SOC devices to ensure a safe communication between partner devices with data rates in the multi-gigabit per second range. These I/O features raise test requirements that are well known in the SOC test arena, but are new to memory ATE. On the other hand, requirements that are typical for memory devices such as massive multi-site implementations or single ended semi-duplex data transmission are still present even for memory devices running at multi-gigabit per second data rates. This combination of old and new test requirements results in significant challenges for ATE systems to allow competitive test times and sufficient signal integrity for the complete signal path from the pin electronics front-end up to the DUT.

In this paper, we describe the details of these challenges for testing high-speed memory devices and how they are addressed with Verigy's new HSM6800 pin electronics.

Key Words- GDDR5, DDR3, HSM6800, High-Speed Memory

1. Introduction

The continuously increasing need for memory bandwidth was mainly addressed by increased I/O data rates of the memory devices in the past. This data rate increase for memory devices results in different challenges depending on the type of memory that is considered. For ultra-high speed memory devices that are used in a well known and well controlled system environment, the challenges are similar to the high-speed I/O interfaces used in the computation area. These challenges are mainly caused by practical design and system manufacturing limitations that exist for the established, cost-efficient materials which are used for system manufacturing (e.g. FR4 as PCB base material). In order to solve these challenges, changes in the timing architecture that are typically more tolerant to the physical material limitations are required. For lower speed memory devices, the existing timing architectures might still be kept, but specification parameter margins get tighter and tighter especially for timing parameters, because the timing budget allocated for the signal path stays constant while the overall timing budget shrinks. From a testing perspective, both of these cases raise new challenges and requirements for the memory ATE that is used to test these devices. In this paper we first want to extract these challenges for a representative of each of the two device groups mentioned. For the ultra-high speed memory components we will analyze GDDR5 and for the lower-speed memory devices we selected DDR3. After an introduction to the HSM6800 pin electronics card

with a description of the new features of this card, we will discuss how these features are used to address the test challenges for GDDR5 and DDR3 that we identified before.

2. High Speed Memory Test Requirements

In this section, we want to discuss the test requirements for the two memory standards that are set to dominate the high-speed memory (HSM) market over the near future. These standards are DDR3 [1] for the high-speed memory mass market and GDDR5 [2] for the lower volume but higher speed HSM market segment. Currently, the maximum specified data rate for DDR3 is 2.133 Gbps [1]. For GDDR5, the JEDEC specification does not specify distinct data rates, but device manufacturers have prototype devices running up to 7 Gbps [5]. It is important to note that we won't give a complete overview of these interfaces but concentrate on the key test challenges only.

2.1. DDR3

DDR3 employs an at-cycle source synchronous interface for the data transmission on its high speed pins. The at-cycle source synchronous interface consists of the differential timing reference signal DQS/DQS# and the single ended data byte pins DQ0..DQ7 for the x8 device configurations that are predominantly used. The test challenge with at-cycle source synchronous interfaces is that the setup and hold times of the data signals (DQ) are not related to an absolute timing instance, but to a signal (DQS) that might vary over time.

Moreover, the setup and hold time parameters of at-cycle source synchronous interfaces are typically the timing parameters with the tightest timing specifications. The (potentially) dynamic movement of the timing reference for the setup and hold times during the pattern execution has a twofold consequence for testing at-cycle source synchronous interfaces.

Firstly the measurement of the setup and hold times itself is a challenge because for each instance in the pattern, not only the position of the respective data edge on the DQ pins has to be measured, but also the corresponding reference edge on the DQS signal. This makes it impossible to do the setup and hold time measurement with a global search function as it can be done for interfaces that have a fixed timing instance, the setup and hold times are referenced to.

Secondly, the dynamic movement of the whole data bus can cause the functional tests to fail if the amount of movement is large enough to shift the open data eyes of the DUT signals beyond the fixed compare strobes of the ATE.

Another test challenge with DDR3 is reflected by the jitter specifications that have to be guaranteed for the central reference clock signal. Note that the DDR3 jitter specification as defined in [1] allows for multiple interpretations and is contradictory within itself as it is given in the standard. The jitter description given in this paper is one of the possible interpretations of the specification. These jitter specifications are separated into three main categories. The first category is defined by the parameter $t_{JIT(per)}$ and defines the jitter on the clock period the device has to tolerate between any rising clock edges within 200 clock cycles. The second jitter category is the cycle-to-cycle jitter the clock device has to tolerate from one rising clock edge to next rising clock edge. Consequently, with the 'any out of 200 cycle' requirement for $t_{JIT(per)}$, this parameter is $t_{JIT(cc)} = t_{JIT(per,max)} - t_{JIT(per,min)}$. The last category defines an n-th cycle accumulated jitter function. This function is defined by minimum and maximum jitter that can occur from the rising edge of the clock on a reference cycle to the rising edge of the clock in the n-th cycle after the reference cycle. The values defined for this function span over 50 cycles. If the min and max values specified for the 50 cycles are combined to the jitter modulation function they define, the modulation waveform shown in Figure 1 is obtained. The cycle time of this waveform is 100 times (50 cycles for max jitter values and 50 cycles for min jitter values) the cycle time t_{CK} of the device reference clock.

In principle, the specification of the jitter in the form of the n^{th} cycle jitter defines the amplitude of the jitter that has to be tolerated for distinct jitter frequencies with an increase in the allowed jitter amplitudes for a decrease of the jitter frequencies.

The challenge with the verification of the jitter specifications first of all is to generate all of the required types of jitter on the CK driver signal of the ATE. Another challenge is that an ATE has to be able to execute the jitter tests in an efficient manner to keep test times at a minimum, which is especially important for production test implementations.

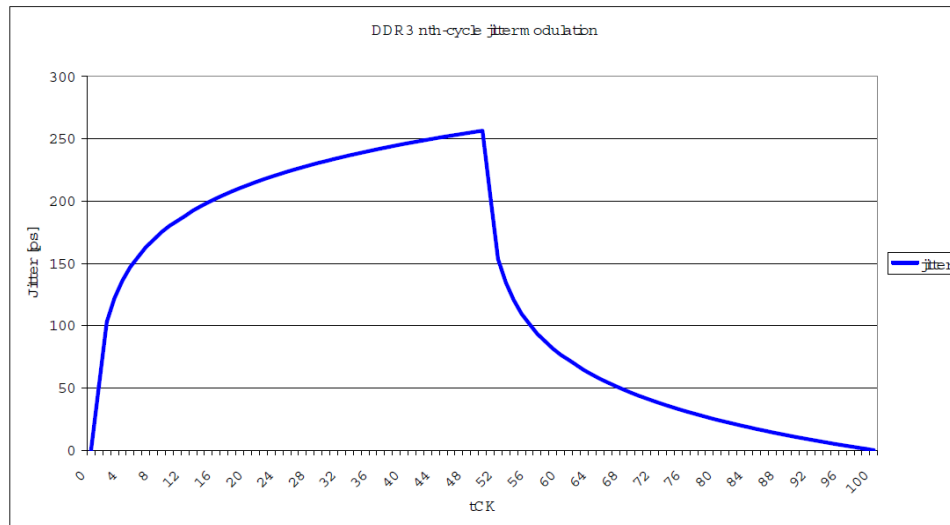


Figure 1. DDR3 n^{th} cycle jitter modulation waveform

2.2. GDDR5

GDDR5 uses a forwarded clock interface that requires extensive device training [3][5][6][7]. The training steps are separated into an optional address training that aligns the address signals to the central device reference clock, a clock training that aligns the forwarded clock signals to the central reference clock, a read training and a write training. The read and write trainings ensure that the DQ data eyes for read and write operations have optimum timing margins on the GDDR5 device and the memory controller side (the ATE system in the case of a test environment). The training is completely controlled by the ATE and all required timing adjustments for the required training step are done on the ATE. The challenge with these training steps is that besides a few command pins and the central reference clock signal, all other pins of the device undergo an identification of the target timing and the re-programming of the timing to this target for each pin. It is important to note, that each of the trained pins will end up with an individual timing that needs to be set for that pin which makes global handling of pins as groups during the training impossible.

The second test challenge we want to consider in this paper is similar to the dynamic timing movement of a DUT we mentioned already for the at-cycle source synchronous interface of DDR3. GDDR5 with its forwarded clock interface also can exhibit such a behavior. The ATE needs to be able to follow such movements that might occur on the DUT in order to guarantee a correct functional test of the DUT. The fact that GDDR5 uses a forwarded clock with device training instead of an at-cycle source synchronous timing architecture simplifies the test of that interface with regards to setup and hold time verification. Due to the training of GDDR5, it is guaranteed that the device is operated with optimum timing margins and setup/hold times are uncritical parameters. In fact GDDR5 does not even specify setup and hold times on the forwarded clock interface, but only specifies offset boundaries between the data pins and the forwarded clock.

These offset values are relatively relaxed taking the absolute device operation speed into account.

Despite the fact that the GDDR5 specification does not contain any specific parameters for jitter values, jitter characterization is considered an important task for GDDR5 [10]. As for DDR3, the test challenges for jitter characterization of GDDR5 are the generation of stimulus signals with well defined jitter content. The jitter measurement capabilities of the used ATE hardware are also important for the jitter characterization of GDDR5.

2.3. General test requirements

A general test challenge that also exists for non-memory high-speed test applications is the transmission of the signals between the ATE and the DUT. Bandwidth limitations on this signal connection cause frequency dependent loss that manifests itself as inter-symbol interference (ISI) induced jitter at either the ATE comparator for memory read operations or at the DUT pin for memory write operations. ISI can have severe impact on the jitter a device experiences for signals that are stimulated by the ATE and on the measurement results of DUT signals that are tested by the ATE. Another general test challenge for memory test implementations is the number of test sites that can be implemented with a given ATE for a certain application. The maximum parallelism that is achievable with an ATE system is one of the key measures of memory manufacturers to judge the productivity of a test system although this can only be seen as a rule of thumb and detailed cost of test analysis might reveal advantages for lower parallelism than the possible maximum e.g. due to device test time to handler cycle time mismatches.

3. HSM6800 Overview

The heart of the HSM6800 pin electronics card is represented by the next generation of Verigy's integrated test processor. Compared to the legacy HSM3600 pin electronics cards, the new test processor/front end combination contains additional functionality that offers increased test coverage for the devices under test. In this paper we only will concentrate on new capabilities that directly have influence on the test of high-speed memory devices from an application point of view. Other features that for example support improved infrastructure functionality are not in the scope of this paper.

3.1. Hardware Overview

The HSM6800 cards follow Verigy's proven and well established water cooled mechanical architecture around a cooling plate that guarantees a controlled temperature environment for the core components of the pin electronics card. As the name HSM6800 already suggests, this controlled environment allows data rates up to specified 6.8 Gbps. A picture of the HSM6800 card is shown in Figure 2.

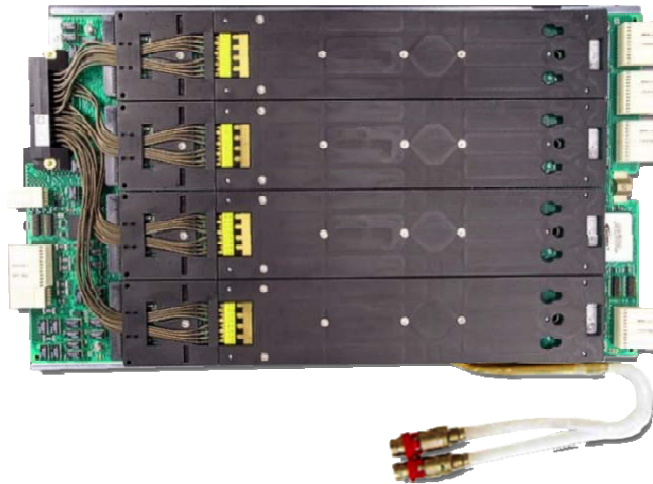


Figure 2. HSM6800 channel pair structure

The highly integrated mechanical architecture together with further electrical integration of the test processor allows for a channel count of 64 channels per card. All of the channels can operate in semi-duplex bidirectional manner within the full specified data rate range.

3.2. HSM6800 Test Features

The new hardware-supported test features of HSM6800 are distributed between the digital multi-core test processor and the front end pin electronics chip that shapes the stimulus and measurement signal in the analog domain.

The function blocks that are relevant for memory test application we consider in this paper are the jitter injection capabilities, embedded search support, transition tracking, simultaneous bidirectional operations and programmable signal equalization.

3.2.1. Jitter Injection

As discussed in Section 2, state-of-the-art memory devices require proper jitter characterization to guarantee correct device operation. For the jitter measurement, the well known and efficient methodologies available already for previous HSM pin electronics cards [11] are also applicable for HSM6800. In addition, HSM6800 now allows users to generate jittery stimulus signals in a convenient way. HSM6800 offers modulation capabilities for the edge control delay lines that allow the selection of modulation functions from a pre-defined set (e.g. sinusoidal, rectangular ...) or the definition of arbitrary modulation waveforms by the user. Besides the modulation function itself, the frequency and amplitude of the jitter modulation function needs to be defined by the test engineer. All jitter injection controls are easily accessible via test method API calls. Especially the arbitrary waveform capability allows a test engineer to also cover jitter modulation characteristics that do not follow a common standard such as for example the n^{th} cycle jitter profile defined by DDR3.

An example for a typical jitter measurement that requires jitter injection during device characterization is the acquisition of a jitter transfer function. For GDDR5, such a measurement characterizes the jitter/frequency behavior of the (optional) PLLs that are driven by the forwarded clock signals (WCK). For the jitter transfer measurement, jitter modulation is applied to the WCK clock signals. The device is set up to drive a clock signal on its DQ pins for which the timing is defined by the jittery WCK clock after being transferred through a PLL as shown in Figure 3.

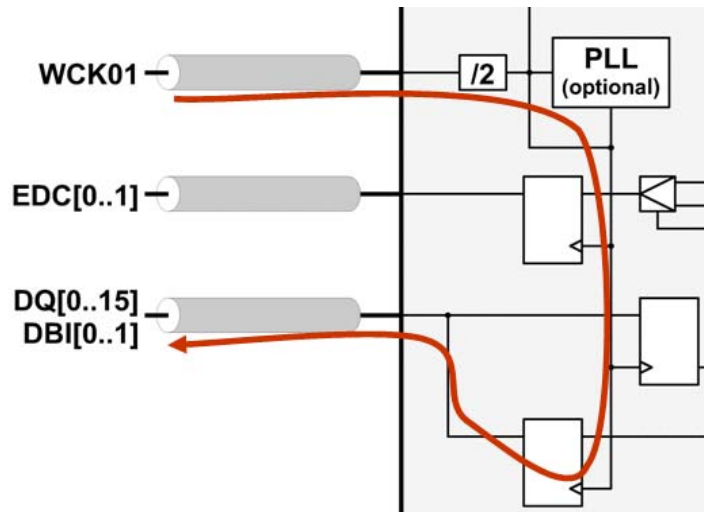


Figure 3. Jitter transfer measurement path for GDDR5

Measuring the jitter for increasing jitter modulation frequencies on the DQ pins and putting it in relation to the jitter injected on the WCK signal allows to assess the jitter transfer function of the PLL.

3.2.2. Embedded Searches

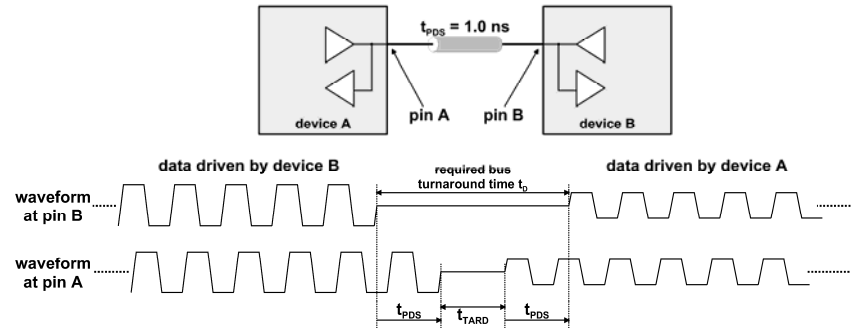
As mentioned in Section 2.2, device training requires a per pin identification of the DUT data eyes and an adjustment of the ATE timing to these data eyes. Traditionally, such a task was implemented using timing searches and timing re-programming that was controlled by the workstation connected to the ATE. With the individual timing that needs to be identified and set per pin for the majority of DUT pins and over dozens of sites in memory test implementations, such an approach is not feasible anymore in a production environment because the required communication between ATE and control workstation slows down the performance of the training significantly. With HSM6800, embedded searches are possible that are entirely controlled by a microcontroller core on each test processor. In order to initiate such an embedded search, the search parameters are passed to the per-pin embedded microcontrollers. Once the microcontrollers of all pins to be searched obtained their parameter set, the search is started and each microcontroller autonomously executes the search algorithm independently of the other pins that are searched. All search iteration settings and decisions on the direction and stepping of the next search step are done locally for each test processor by the embedded microcontroller. This local control of the search and the timing-adjustment to the final search result allows true parallel execution of device trainings without the need for any communication during the training between the central control workstation and the single test processors. This speeds up device training dramatically and allows production worthy device trainings per pin over the typically very high site counts seen in memory applications.

3.2.3. Simultaneous Bidirectional

The challenge with semi-duplex bidirectional interfaces, which are typical in the high-speed memory arena, is the fact that the propagation delays between an ATE pin electronics and DUT are much larger than is the case for a memory-controller to memory connection in a system. Of course the minimum bus turnaround times that are specified for memory devices are oriented on the final system environment the memory device will be used in. If these minimum bus turnaround times are to be tested on an ATE, the longer propagation delay times result in a data collision on the ATE-to-DUT connection. This is due to the fact that the specified bus turnaround time at the DUT is realized with the ATE driver already sending data while there is still data

stemming from the DUT on the connection in order to compensate for the longer propagation delay time on the ATE to DUT connection. The colliding data however cannot be compared reliably anymore to the expected data in the ATE receiver as shown in Figure 4.

SYSTEM ENVIRONMENT



ATE ENVIRONMENT

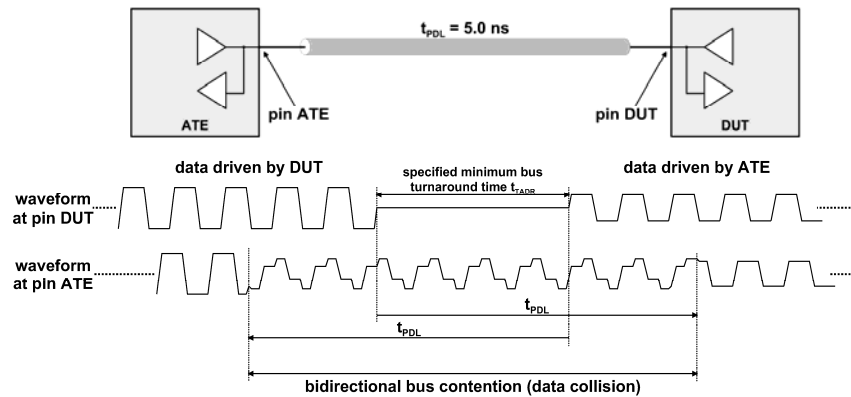


Figure 4. Data collision at ATE receiver when testing minimum bus turnaround times for semi-duplex data connection; from [3]

In the past there were two possibilities to handle such a situation. The first option was to test with relaxed turnaround times to avoid data collisions on the semi-duplex signal connection. This however has the drawback of potential test escapes and increases the test execution time due to the extended turnaround times. Another commonly applied option was the use of dual transmission line (DTL) connections instead of single transmission lines (STL). This in fact transforms the bidirectional signal connection from a semi-duplex connection into a dual-simplex connection without the potential for data collisions at the ATE receiver. The drawback of the DTL solution clearly is that separate ATE driver and receiver channels are required to implement the DTL topology. This reduces the maximal available site count for a given real estate.

HSM6800 contains simultaneous bidirectional (SBD) signal handling capabilities to overcome these restrictions. The SBD correction circuitry in the HSM6800 receiver part of the bidirectional channels allows the correction of the data collision effect on an STL connection. For this correction, the signal of the ATE driver that is known is used to compensate the received signal that is distorted due to the data collision. After the compensation, the signal that originally was sent by the DUT is available and can be compared to the expected data in the HSM6800 receiver section of the bidirectional channel. This way SBD allows full testing of minimum bus turnaround times on STL connections without sacrificing site count due to DTL usage. The effect of the SBD

functionality for a semi-duplex bidirectional signal that is tested with its specified minimum read-to-write bus turnaround time is shown in Figure 5.

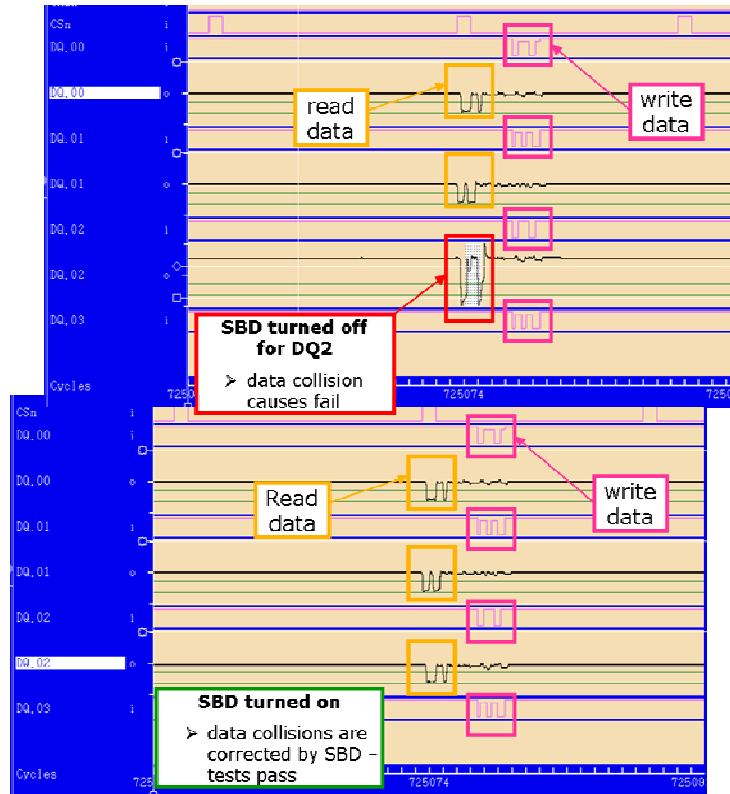


Figure 5. Semi-duplex bidirectional signal waveform at ATE receiver without SBD and with enabled SBD functionality

3.2.4. Programmable Equalization

The last feature of HSM6800 to be discussed here is the programmable equalization that is available separately for HSM6800 drivers and receivers. Equalization is a methodology to compensate for frequency dependent loss on the connections between the ATE and the DUT that causes ISI jitter at the DUT and ATE receivers. A detailed description of equalization and its implementation in the HSM6800 channels can be found in [9]. For HSM6800 the frequency depended loss can be compensated separately for drivers and receivers. In the level equations of the HSM6800 channels three compensation factors are available that address high frequency (V_{PP}) mid frequency (V_{PM}) and low frequency (V_{DC}) loss as shown in Figure 6. The waveform generated by the ATE driver and received by the ATE comparator can be adjusted with the use of these parameters in a way that the signal at the DUT is not affected by the loss of the test fixture connections between ATE frontend and DUT pins.

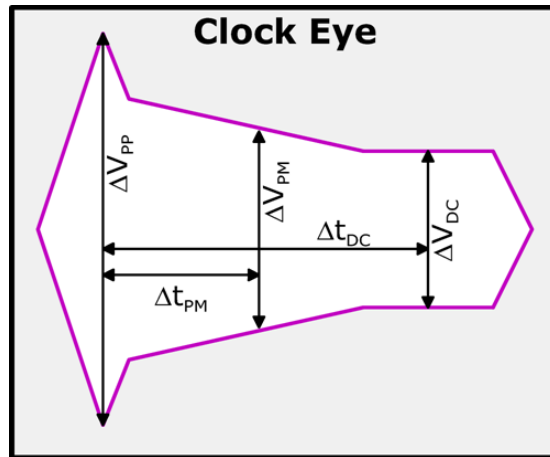


Figure 6. HSM6800 equalization parameters V_{PP} , V_{PM} and V_{DC}

Besides loss compensation, the equalization parameters also can be used to increase frequency dependent loss at the ATE frontend. The possibility to have this option allows the emulation of connections with low analog bandwidth in a system environment. Thus, the reaction of a DUT to such an environment can be tested on the ATE. With such a reduced bandwidth setting, for example, ISI at a DUT receiver can be generated that reflects a typical system transmission line rather than a perfectly matched connection. The signal shapes at the ATE pogo for maximum and minimum settings of high frequency equalization parameter of the ATE driver is shown in Figure 7 for a falling signal edge.

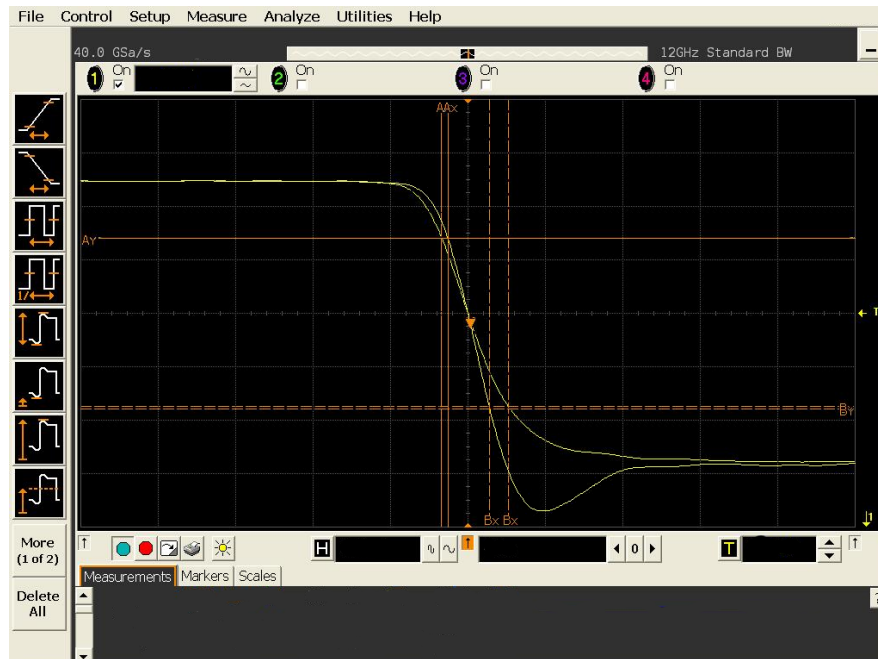


Figure 7. Falling transition signal shape with minimum and maximum setting for high frequency equalization parameter

4. Summary

In this paper we presented the some of the key test challenges that state-of-the art high-speed memory devices pose on high-speed memory test systems with their adoption of advance timing architectures that allow high-speed operation in a system environment. After a short general description of Verigy's new HSM6800 pin electronics card, we mapped the new features of HSM6800 to these test challenges and discussed how these features can be used to address the test challenges.

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