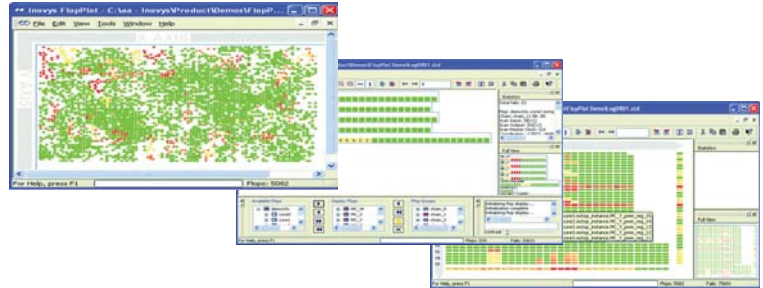


FlopPlot™

Identify and Diagnose Device Problems Faster



A suite of software analysis tools that display multiple views of device failures, FloPlot uniquely links a chip's failure data with its design hierarchy and layout.



Identify and Diagnose Device Design Problems Faster

The challenges in achieving successful debug of new semiconductor designs are compounding, including: Increasing gate count & density; New technology nodes; Decreasing external access; and Increasing defect and fault mechanisms. The response to best address these challenges is implementation of Design For Test (DFT) and leveraging structural test methodologies. Large, complex semiconductor devices such as ASICs and SoCs can generate immense amounts of structural test failure data, which can be very difficult to interpret and analyze. FloPlot manages these large volumes of data efficiently and converts them into easy to understand formats and graphical displays. FloPlot provides a powerful suite of software tools that enables DFT, Test, and FA engineers to quickly identify and resolve failures in even the most complex devices that contain millions of gates.

Improve Productivity with Seamless Bidirectional Links to EDA

All commercial EDA Design tools provide ATPG output in the IEEE1450 Standard Test Interface Language (STIL) format. The Stylus™ OS on the Inovys test platforms loads and executes STIL files directly without additional translation steps. This process is automatic, immediate, and maintains the integrity of the original design database. When failures are detected, FloPlot can map every failure to a flip-flop and pattern for fast analysis and then link back to ATPG diagnostic tools to identify faults down to the gate-level.

Enhanced Failure Analysis Capability with Unique Fault Filtering

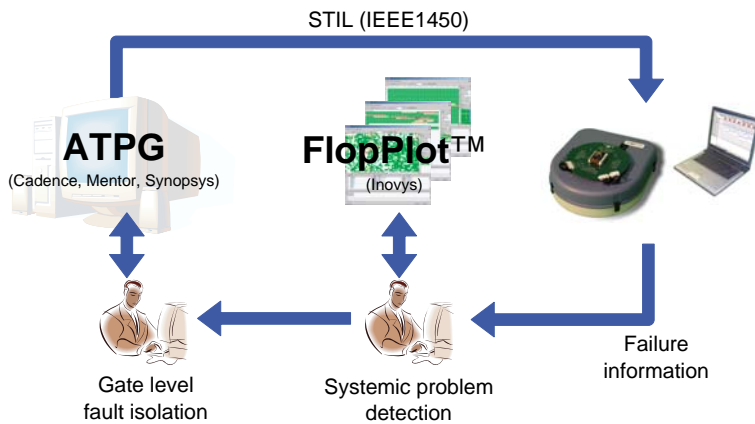
ATPG diagnostics typically operate on the single fault assumption: If the device has many failures the diagnostics algorithms quickly break down and the failures cannot be identified. FloPlot significantly enhances diagnostics capability by providing comprehensive fault filtering mechanisms such as hierarchical, scan chain, pattern, etc. These fault filtering mechanisms reduce the number of faults that the diagnostics tool has to analyze – enabling the successful diagnosis of devices which could not be achieved by other methods.

Key Benefits:

- Identify and diagnose device design problems faster
- Improve productivity with seamless bidirectional links to EDA
- Enhanced failure analysis capability with unique fault filtering
- Efficient data analysis through hierarchical displays
- Accelerate yield learning with instant mapping

- Identify DFT failure patterns in first silicon faster and easier
- Identify gate-level faults by linking to diagnostic tools from Cadence, Mentor Graphics and Synopsys
- Track and review failures by lot, wafer, individual die
- Increase yield by systematically identifying failure distribution

Identify and Diagnose Device Problems Faster

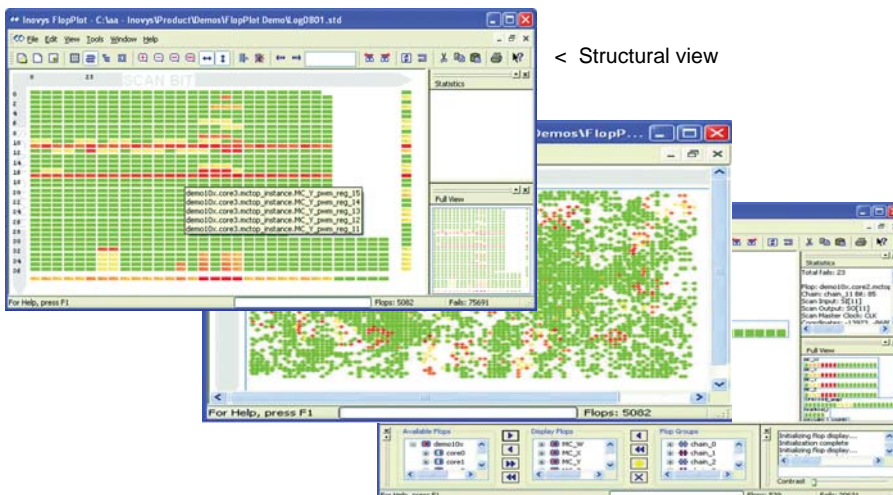


Efficient Data Analysis Through Hierarchical Displays

Failing flip-flops in a device can be identified by scan chain using “Structural View” within FlopPlot. Structural test results generate complete pattern, chain, and bit information for better problem solving and fast debug. A scan chain fault, such as a hold-time violation, has a unique telltale signature. When viewed graphically in “Structural View” this alternating pattern of bit failures is clearly highlighted. The “Hierarchical View” mode within FlopPlot enables users to view failures by functional behavioral blocks – starting from a core-level and zoom down to the lowest-level design module. Once a filter is applied, FlopPlot can transform and display the same information as scan chain data (the “Structural View”) or as a relative die plot (the “Physical View”).

Accelerate Yield Learning with Instant Mapping

FlopPlot leverages structural test data by using physical layout information to generate physical failure maps. DFT and Test engineers can use this graphical view to immediately analyze defect clusters and so identify failures by occurrence and impact. An iterative process of elimination can then be followed to resolve each problem in turn. This significantly reduces the demands of time needed on production and laboratory equipment and on the test engineer’s time – always a precious commodity. This enables production yield ramps to be achieved in the most efficient manner possible.



SPECIFICATIONS

Import and View Structural Test Data

- Structural view: By scan-chain structure
- Hierarchal view: By design architecture
- Physical view: By physical layout

Track & Filter by Multiple Fail Variables

- Structural test: Scan chains, bits in chain, scan patterns, pattern set, etc.
- Manufacturing: Program rev, lot ID, wafer ID, facility, XY coordinate, etc.
- Pattern content: Execs, bursts, specs, test IDs, etc.

Powerful GUI for Visual Variables

- Zoom to any level of detail within View
- Adjust color thresholds to filter failures by numerical intensity
- Intuitive displays show complete design data on any hierarchy or bit cell

Direct Links with Leading ATPG Tools, including:

- Mentor Graphics FastScan™
- Synopsys TetraMAX™
- Cadence Encounter™

PC-Based with UNIX Links

- Inovys DiagLink™ connects FlopPlot to UNIX-based ATPGs
- Automated scripts enable remote management of long diagnostic jobs via CygWin interface
- Runs on any Win2K or WinXP PC