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REDUCING RISK

By Paul Sakamoto, EE Times
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Midyear forecast 2004

Although the general economy appears to be improving this year, a risk-adverse mentality continues to affect the scope and timing of many decisions.

One result is that many foundries are operating at greater than 90 percent of capacity. This is simply too high to effectively respond to any further positive market growth. EE Times recently reported that lead times at IBM's fabs are now pushing six months — a veritable lifetime in the cutthroat ASIC businesses.

Manufacturers of deep-submicron ASICs and systems-on-chip are also dealing with extreme complexity, lower operating voltages and smaller geometric features. While all of those advances offer many benefits, they also create new classes of defects, faults and failure effects, making it harder than ever for manufacturers to meet quality and reliability requirements.

Add on the high cost of masks, approximately $500,000 to $1,000,000 per design, and you have a situation where the pressure is higher than ever to get silicon right the first time. Within this environment, any bottleneck in the conventional chip design and test process is under close scrutiny. Semiconductor makers must implement more efficient methods to reduce the inherent risks associated with each stage of the design and manufacturing process.

More chip companies are taking advantage of design-for-test methodology, in which diagnostic and test circuits are inserted into the chip design. DFT primarily allows full fault coverage of very complex devices. A new and exciting DFT benefit is that when it is paired with the proper equipment and software, it opens the "data wall" that has traditionally existed between EDA and ATE systems, facilitating bidirectional information flow without translation between the two different worlds.

The efficient way to utilize DFT techniques across a broader portion of the semiconductor development process is to use equipment specifically designed for structural test methodologies, which verify a semiconductor's internal circuits rather than its functional behavior. When companies follow a well-planned, comprehensive approach that spans design to production, the synergy of mapping design information against test feedback produces major productivity gains.

By utilizing test hardware and software optimized for structural test and DFT, chip companies can now slash their silicon debug and validation time from weeks or months down to days. High-quality, "known-good" test vectors are a direct output of the EDA suites and can be used to rapidly and productively debug engineering samples. These same vector sets can then be immediately released for production test — a huge engineering productivity enhancement. Once in place, the tools can easily perform gate-level failure analysis on production parts to increase yields.

Structural methodology's "develop once, use many" approach allows risk to be addressed earlier in

the IC development process, where it can be managed more efficiently. By investing a small percentage of die area in DFT and utilizing structural test systems, manufacturers can now reach final tapeout faster, reduce the need for massive amounts of test capital and improve chip yields. And in today's risk-averse economy, even one week of extra time-to-revenue can make a significant difference to any business.

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