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Ac scan needed for nanoscale device testing

By Alfred L. Crouch, EE Times
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Huge transistor counts, rising on-chip clock rates, the relentlessly escalating levels of integration in systems-on-chip, and the new types of defects seen in deep-submicron and nanometer processes are forcing IC design and test engineers to reevaluate traditional approaches to test. Can designers afford to develop functional vectors for 20+ million-gate SoCs that combine multiple functional blocks in processes that integrate anywhere from 90k to 150k gates per square millimeter?

In an increasing number of cases, the answer is no. The development cycle is too short, the task of generating and measuring vectors too complicated, the chip clock rates too high and the test equipment too slow or too costly to execute functional patterns as needed. Most important, the types of defects are changing. In today's nanometer-scale processes, speed-related defects begin to dominate failures. Delay is now the predominant failure mode. Traditional debug approaches cannot detect subtle delays or isolate them correctly.

Timing advantage

Ac scan can be used to accomplish many of those goals. This meth-odology uses scan-based techniques to conduct an at-speed sample cycle for the purpose of verifying timing compliance. The scan shift is performed exactly the same as with dc stuck-at scan; in fact, the scan architecture can be the same. Unlike stuck-at dc scan, however, ac scan conducts sample/capture with the correct timing relationship between a state/next-state vector pair. It can be used to verify frequency compliance, pin specification compliance and manufacturing-induced delay defect content.

Ac scan offers a number of key advantages over traditional functional test approaches. It reduces clocking requirements, eases timing diagnostics and simplifies binning. The vectors generated in ac scan are more efficient than those used in functional test, resulting in a fewer number of them and shorter test times. Moreover, those vectors, automatically generated by automatic test pattern generation (ATPG), are highly portable, a key advantage in any design using embedded intellectual-property blocks.

In addition, since ac path scan vectors are generated against critical paths, they provide a more deterministic result and target more subtle timing. Finally, by eliminating the need for highly precise signal timing and edge placement, complex sequencing capability and high-frequency data rates, ac scan reduces the functionality requirements for automatic test equipment and, ultimately, its cost.

Those advantages don't come free, of course. Ac scan requires that design-for-test (DFT) be inserted on-chip. The strategy implies a silicon cost and also requires that designers rigidly adhere to design rules for test. Finally, it assumes that designers will integrate into their development schedule the time it takes to add DFT and ATPG. While that effort is offset by the saving of time traditionally spent in the post-design phase, this up-front investment in time and cost is not trivial.

By leveraging DFT and ATPG, ac scan can offer a more work- and schedule-efficient test strategy with a more deterministic result. In the process, it can help design teams meet their time-to-market goals and production teams meet their time-to-yield and time-to-volume targets.

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