

# Ocelot ZFP

Accelerate the Path to Profit



An industry breakthrough in semiconductor production test, the Ocelot ZFP leverages DFT methods to maximize efficiency and enable cost of test to scale with Moore's law.



## Accelerate the Path to Profit by Eliminating the Design to Test Bottleneck

Achieving a profitable product in the dynamic semiconductor market today requires overcoming many challenges to get devices into volume production as fast as possible. These challenges include increasing device complexity, shorter product lifecycles and intense cost competition. The best response to address these challenges is implementation of Design For Test (DFT) which includes structural test methodologies. The Ocelot ZFP leverages the key elements of DFT to reduce design debug from weeks to hours and provides the shortest path to high volume production. Architected around the IEEE1450 STIL standard, the Ocelot ZFP is simple to use, has a short learning curve and enables customers to typically be productive within one day. This platform provides seamless bidirectional interfaces between ATE and EDA — including the latest tools from Cadence, Mentor Graphics, Synopsys and others. These attributes eliminate the design to test bottleneck and accelerate the path to profit.

## Maximize Production Efficiency and Yield

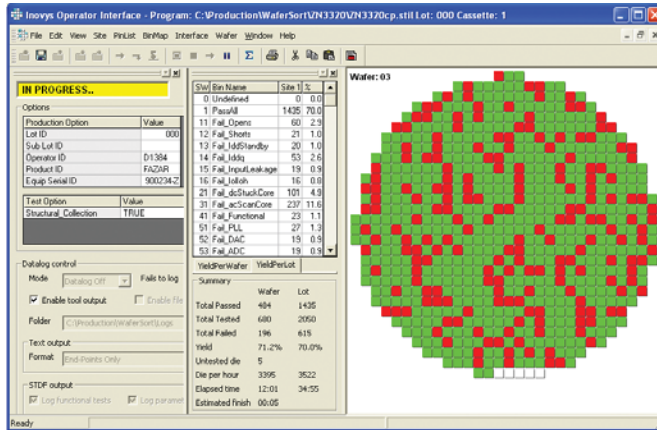
The new generation of complex System on Chip (SoC) devices are getting harder to test due to increasing gate count and density, new technology nodes, decreasing external access, and increasing defect and fault mechanisms. The Ocelot ZFP addresses these new test challenges with an optimal combination of functional and structural test capabilities. Structural testing of complex SoCs requires larger pattern memories, internal delay testing, advanced failure capture and analysis capabilities — all of which traditional testers either lack or are too cost prohibitive. The Ocelot ZFP optimizes fault coverage resulting in maximum production efficiency and maximum yields.

## Key Benefits:

- Accelerate the path to profit by eliminating the design to test bottleneck
- Maximize production efficiency and yield
- Achieve the lowest cost of test
- Slice weeks from test program development
- Isolate speed defects using AC Scan

- Zero Foot Print (ZFP) fits within any prober form factor
- Up to 512 bidirectional I/O pins
- Up to 32MB of real-time fail/data capture memory per pin
- 400MHz clock channels for precise transition and path delay measurements
- Stylus® Operating System (compliant with IEEE1450 STIL)

# Accelerate the Path to Profit



## Achieve the Lowest Cost of test

The performance and price of traditional functional only testers, by definition, are locked into the performance of the device being tested. Structural test breaks free from this treadmill and enables the use of more efficient, therefore, lower priced test platforms. The Ocelot ZFP leverages structural test to meet the requirements of multiple device generations, preserving capital investment and scales with Moore's Law. In addition to lower acquisition and maintenance costs, the Ocelot ZFP has the lowest operating cost requiring no floor space and power consumption that is a tenth of traditional test systems. Combined with the significant efficiency gains in both engineering and production, the Ocelot ZFP provides the lowest cost of test.

## Slice Weeks from Test Program Development

Test programs are automatically and immediately generated from the ATPG output of the EDA tools using native STIL — eliminating the time consuming and error prone translation process required by all proprietary test languages. Test vectors and programs can be quickly developed and debugged on the Ocelot ZFP, including powerful tools for Scan test debug. Typical test program generation and debug effort is reduced from more than four weeks to a few days.

## Isolate Speed Defects using AC Scan

New sub-90nm designs exhibit new fault models which include both stuck-at and speed related. The High Performance Clock Channels (HPCC) in the Ocelot ZFP enable AC performance testing up to 400MHz or even higher using the device's internal PLLs. The Ocelot ZFP is complemented by a comprehensive suite of AC Scan tools which provide in depth analysis of the distribution of AC performance across individual design elements, highlighting path delay and transition delay faults. Now, speed defects can be isolated using the unique AC Scan capability.



## SPECIFICATIONS

- Up to 512 bidirectional I/O pins
- 50MHz data rates
- 400MHz high performance clock channels
  - AC Scan dynamic waveform switching
  - Free running BIST
- Dynamic Data Matrix™
  - Extended scan depths up to 4GV
  - Flexible memory remapping
- Up to 64Mv pattern memory per pin
- Up to 32M of capture memory per pin
  - Full tester rate data capture
  - Fail Capture or Data Record modes
- PMU per 64 pins, switchable to any pin
  - -2V to +5V voltage range
  - 10µA, 100µA, 1µA and 40µA current ranges
- Frequency measure up to 200MHz
- Standard prober and handler docking interfaces
  - Direct probe card docking
- STYLUS® tester operating system