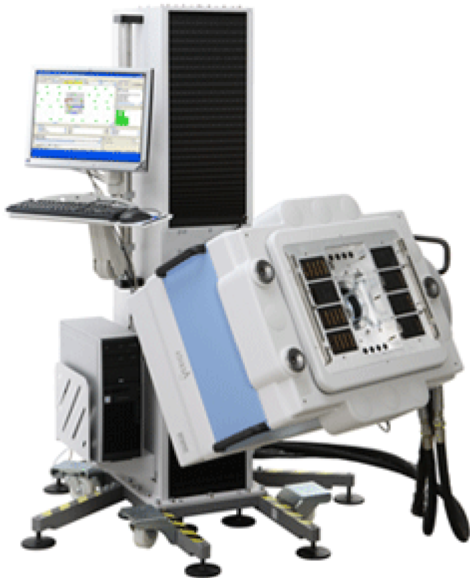
Inovys Silicon Debug Solution for the V93000

Solution Overview



The Inovys Silicon Debug Solution combines the revolutionary Inovys FaultInsyte software with the Verigy V93000 SOC test system to deliver an integrated solution that enables rapid detection and diagnosis of electrical failures on complex SOC devices. This significantly shortens time to debug, ramp and volume production.

Industry Challenges

The rapid pace of innovation has created powerful SOC solutions at consumer prices. This has created a highly competitive market place where billions of dollars can be won by the right design delivered at the right time. These new designs are produced on processes that challenge the fundamental laws of physics and are highly sensitive to equipment variation.

The industry now produces new designs in a complex world where process and design interaction have created new complex failures that stand in the way of billion-dollar opportunities. These interactions lead to new types of defects such as blocked chains, which create noise in the debug/diagnosis process. They also lead to new types of design issues such as delay defects in combinational and sequential logic.

The challenge is made even greater by the growing complexity in device structure and design techniques.

Multiple design organizations use multiple IP blocks and multiple libraries that need to work together throughout the process window, often across multiple fabs.

These new challenges come at a time when product lifetimes are shrinking, leading to pressure to reduce time for debug and characterization activities. These problems are seen for the first time at first silicon.

Solution Summary

Rapidly detect, diagnose and visualize electrical failures on complex SOC devices shortening time to debug, ramp and volume production.

- Accelerate the time for defect detection and diagnosis by efficient mapping of electrical failures to physical defects using logic bitmaps.
- Uniquely find certain elusive defects while the device is on the tester.
- Enable efficient collaboration between design and test through an integrated toolset.
- Improve productivity and utilization of installed V93000 systems.
- Leverage key learnings from best-in-class industry techniques and methods in a standard toolset and test program development

The Inovys Silicon Debug Solution is a suite of tools that provides a comprehensive

solution that decreases the time previously needed for defect detection and diagnosis by efficiently mapping electrical failures to physical defects through logic bitmaps.

The Silicon Debug solution uniquely finds certain previously elusive faults while complex SOC devices are still on the tester. The solution enables the ability to efficiently collaborate between design and test through an integrated toolset. It also successfully leverages multiple key learnings obtained from best-in-class industry techniques and methods and consolidates them in a standard toolset and test program development.

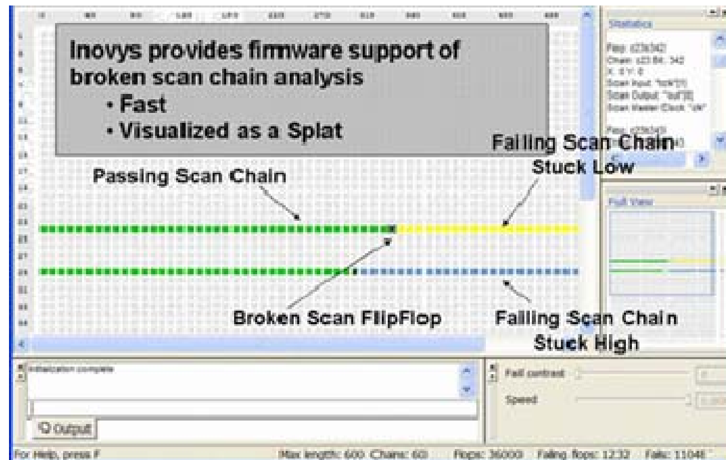


Fig. 1: FaultInsyte provides high-speed automated localization and analysis of hard to find faults such as blocked chains and hold-time faults (Vddmin problems) in chains.

Requirements and Solution Summary

Requirement	Solution
Solution to cryptic ASCII based datalog files	Inovys FlopPlot's unique wafer, die and scan-based failure visualization tools
Improvement to tester-centric pin and cycle count format	On-tester conversion to pattern, chain and bit • In the language of the designer • In a design hierarchy context • With accurate x, y die coordinates
Layout extraction	Lightweight net trace from failing flip-flop providing cell and routing level visualization of failures
High-speed, on-tester solution for determining chain faults	On-tester chain failure localization to chain and bit • For blocked chains • For hold-time (Vdd min/max) faults
Protection for design IP	IP Protected Splats™ • Client-server type interface to allow communication between the fabless company and the foundry that provides enough information to solve the problem without compromising IP
Link to EDA tools	Import/export solution to EDA tools from Cadence, Magma, Mentor Graphics and Synopsys
Within-die performance analysis tools	Shmoo at every flip-flop • Using on-chip PLL or off-chip clocking • Visualized within the FlopPlot framework
Ease of use	Award-winning graphical user interface (GUI) that allows any DfT, failure analysis (FA) or design engineer to say, "I can use it myself!"
More power domains	Verigy DC Scale DPS32 card enables testing of 32 power supplies per card; multiple cards are available, limited only by number of slots available in the test head
DC to Gigabit I/O	V93000 architecture scalability allows uniquely wide range of test methodologies and applications for debug, characterization, and high volume manufacturing
Megabits of embedded RAM	V93000 Memory Test Plus (MTP) module allows testing in native or scan-based mode
Accuracy, stability, repeatability and reliability, flexibility and scalability	Proven V93000 architecture delivers

Features and Benefits

The Inovys Silicon Debug Solution for the V93000 provides proprietary fault-targeted approaches to localizing failures in real time (while the part is still on the tester) to more efficiently debug new devices and accelerate time to volume production. Its key component, FaultInsyte, provides the most complete approach for systematic and parametric fault localization in the industry, on the industry's premier SOC tester, while reporting actionable information back in the language of the designer.

New, complex SOC designs can now be accelerated through the debug and production process by interrogating on-chip DFT structures with structural test methodologies running on more efficient test systems. The Silicon Debug solution combines the revolutionary Inovys FaultInsyte software with the Verigy V93000 SOC test system to display structural, hierarchical and physical views of DfT failures. It is the first tool that can link a chip's failure data with its design hierarchy and layout. These capabilities allow the analyst to interpret first silicon data in minutes.

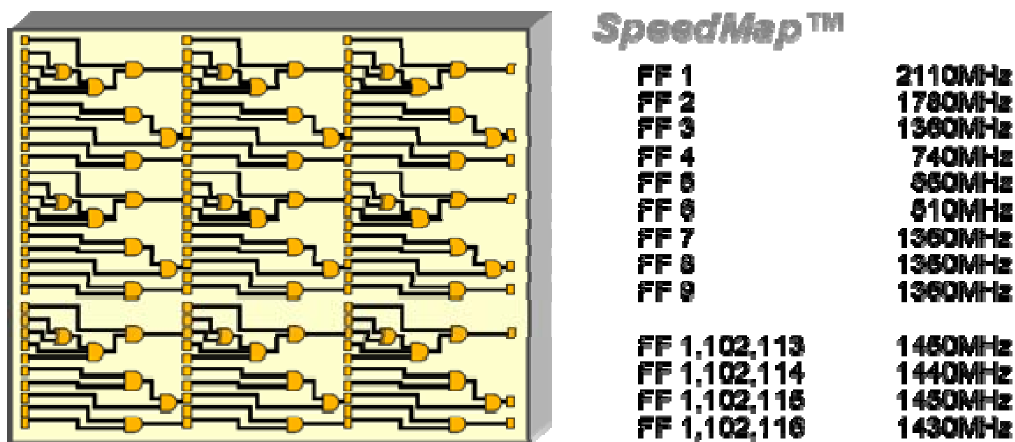


Fig. 2: How fast are the parts? How big is the performance process window? Which circuit elements limit performance? Let FaultInsyte help you exceed your limits.

	Feature	Benefit
FaultInsyte	STIL environment	Increase productivity by leveraging the STIL standard. Includes real-time updates of EDA modules without reload.
FaultInsyte	ATPG link	Minimize data transfer errors with robust bi-directional links to EDA tools.
FaultInsyte	Bare-metal V93000 control	Simple 'user master control' with no test program preparation in SmarTest required.
FaultInsyte	Complete visualization toolset	Immediately see the failure in Structural, Hierarchical or Physical View. Efficiently map failure to physical defect in Advanced Layout.
FaultInsyte	Fault analysis and localization	Detect and diagnose elusive new failure mechanisms in smaller geometries – including blocked scan chains and hold-time faults.

FaultInsyte	IC performance characterization	Identify path-delay and transition-delay faults, characterize AC paths and highlight device to device variations across process corners.
FaultInsyte	Wafer-level debug	Accelerate silicon debug by enabling diagnosis at the wafer level and providing volume data learning.
FaultInsyte	Single DUT interface board	Faster DUT bring-up time with single interface to design and debug. Use the same interface for production test.
FaultInsyte	Stylus operating environment	Immediate effective use with award-winning, simple to use, intuitive GUI. Design and DFT engineers can drive the tool.
FaultInsyte	Leverage V93000 systems	Significantly increase the utilization and performance of installed systems; common platform for engineering and production.

	Feature	**Benefit**
Pin Scale 400	100 Mbps entry level up to 533+ Mbps per pin	Greater flexibility by covering majority of broad side-access pins through majority of interfaces.
Pin Scale 400	64 channels per card	Enables greater multi-site with minimal infrastructure.
Pin Scale 400	Per-pin / per-port / per-site fail log capability	Greater throughput from maximum parallelism.
Pin Scale 400	Selective log of FAIL location per pin/chain	Eliminates "across the bus permutational explosion" of shared resource structure.
Pin Scale 400	True parallel scan fail/bit fail map	Improved throughput.
Pin Scale 400	BIST per pin / per site	Improved throughput from independent interaction.
Pin Scale 400	Xpress data mode	Very fast (1 Gbps) data transfer rate of fail data to workstation.

Key Specifications

Import and view structural test data

- Structural View: By scan-chain structure
- Hierarchal View: By design architecture
- Physical View: By physical layout (wafer or die level)
- Histogram View: Sort by speed

Link to physical layout database

- Provides defect-to-layout overlay
- Trace functions (fan in, fan out)
- Generate IP-protected trace picture (i.e., Splat)

Track and filter by multiple fail variables

- Structural test: scan chains, bits in chain, scan patterns, pattern set, etc.
- Manufacturing: program revision, lot ID, wafer ID, facility, XY coordinate, etc.
- Pattern content: execs, bursts, specifications, test IDs, etc.

Powerful GUI for visual variables

- Zoom to any level of detail within view
- Adjust color thresholds to filter failures by numerical intensity
- Intuitive displays show complete design data on any hierarchy or bit cell

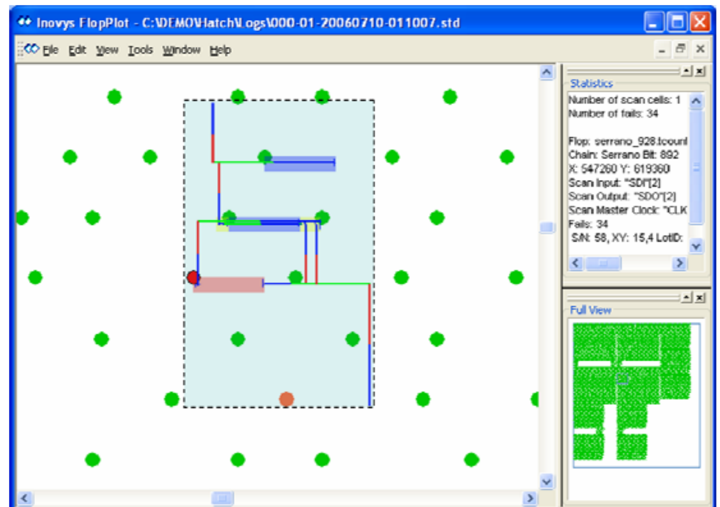


Fig. 3: Splat

Related information

For more information about the Inovys Silicon Debug Solution for the V93000, please visit the following website:

www.verigy.com/go/debug

Contact information

For more information about the Inovys Silicon Debug Solution, please contact your local Verigy sales representative

www.verigy.com/go/contactus

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