

# Personal Ocelot

## The Fastest Path to Device Debug



A powerful and versatile desktop platform for IC engineering and failure analysis.



### Reduce Design Debug from Weeks to Hours

The challenges in successfully debugging new semiconductor designs are compounding, and include: increasing gate count and density, new technology nodes, decreasing external access, and increasing defect and fault mechanisms. The best response to address these challenges is implementation of Design For Test (DFT) and leveraging structural test methodologies. Employing the Personal Ocelot structural test capability can track failures back to individual flip-flops in the design. This is achieved through seamless bidirectional links between ATE and EDA — including the latest tools from Cadence, Mentor Graphics and Synopsys — using the IEEE1450 Standard Test Interface Language (STIL) in native format. This unique combination of structural and functional test capability reduces the typical design debug and validation effort from weeks to hours.

### Optimize Failure Analysis Process

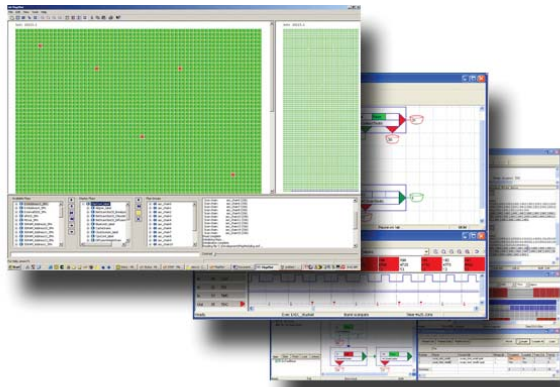
Failure analysis of manufacturing failures or customer field returns can be a difficult and resource intensive task. Now, the time consuming scheduling and setup time of high-cost production ATE is replaced with the compact, low cost Personal Ocelot, located on the engineers desk, and always ready to use. Traditional functional test datalogs failures from outside the device, while structural test datalogs failures from inside the device. The Personal Ocelot can perform both and significantly increases the ability to observe and diagnose the failure. Combining this with the Inovys real-time feedback loop to EDA ATPG diagnosis tools, linked to EDA layout tools, enables precise localization of process and design failures down to the gate level. This results in a significant reduction in failure analysis time and cost.

### Key Benefits:

- Reduce design debug from weeks to hours
- Optimize failure analysis process
- Slice weeks from test program development
- Characterize speed performance down to the design element level
- Improve engineering productivity

- Up to 256 bidirectional I/O pins
- Up to 32MB of real-time fail/data capture memory per pin
- 400MHz clock channels for precise transition and path delay measurements
- DC Parametric Measurement Units (PMUs)
- Stylus® Operating System (compliant with IEEE1450 STIL)

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## Slice Weeks from Test Program Development

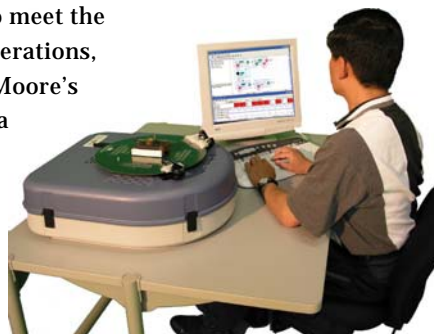
Test programs are quickly generated directly using the output of the EDA ATPG tools in native STIL — eliminating the time consuming and error prone translation process required by other ATE proprietary test languages. In addition, the Personal Ocelot features a comprehensive, industry-leading suite of interactive debug tools. Test vectors and programs can be quickly developed and debugged on the Personal Ocelot, including powerful tools for Scan test debug. These activities can all be performed more efficiently and effectively at the engineer's desk and removes the need to take an expensive production tester offline. Typical test program generation and debug effort is reduced from more than four weeks to a few days.

## Characterize Speed Performance Down to Design Element Level

The Personal Ocelot is a valuable tool for characterizing the speed performance of a new design. Traditional at-speed functional testing only provides the speed characteristics of the design as a whole. Using AC Scan with the Personal Ocelot's AC Performance Package can provide a design's speed performance down to the individual building blocks. The High Performance Clock Channels (HPCC) in the Personal Ocelot enable AC performance testing up to 400MHz as standard. By using the PLLs internal to the device during scan capture cycles this AC performance characterization can be further extended into Gigahertz ranges. The Personal Ocelot is complemented by a comprehensive suite of AC Scan tools which provide in depth analysis of the distribution of AC performance across individual design elements, highlighting path delay and transition delay faults.

## Improve Engineering Productivity

The Personal Ocelot leverages structural test to meet the requirements of debugging multiple device generations, preserving capital investment and scales with Moore's Law. The Personal Ocelot is simple to use, has a short learning curve and allows customers to typically be productive within one day. These attributes result in significant improvement in test engineering productivity while lowering engineering costs.



## SPECIFICATIONS

- Up to 256 bidirectional I/O pins
- 50MHz data rates
- 400MHz high performance clock channels
  - Dynamic waveform switching for AC Scan applications
  - Free running mode for BIST applications
- Advanced Pattern Memory Architecture
  - Up to 64Mv pattern memory per pin
  - Dynamic Data Matrix™
    - Flexible memory remapping
    - Extends scan depths up to 4GV
- Up to 32M of capture memory per pin
  - Full tester rate data capture
  - Fail Capture or Data Record modes
- PMU per 64 pins, switchable to any pin
- Frequency measure up to 200MHz
- Standard DPS: Four 2.5A, 0 to 6V channels
- Optional Power Resource Group adds:
  - One 5A and three 2.5A channels
  - Eight 0.2A, 0 to 16V channels
  - Current measure and programmable current limits
- Uses external PC running Windows XP
  - USB tester interface
- STYLUS® tester operating system
  - Based on STIL (IEEE 1450)
  - Comprehensive suite of interactive analysis and debug tools